BAB V
KESIMPULAN

Dari pembahasan pada bab-bab sebelumnya, dapat diambil kesimpulan bahwa:

1. Alat pengatur yang dibuat dapat digunakan dengan cukup baik pada batasan pengukuran 10 lux sampai dengan 800 lux. Hal ini sesuai untuk keperluan pengujian pada perencanaan pengaturan penerangan tata cahaya, seperti pada tujuan rancangan.

2. Kesalahan alat ukur ini didominasi pada bagian transduser, yaitu terletak pada sensitifitas dan linieritas transduser.

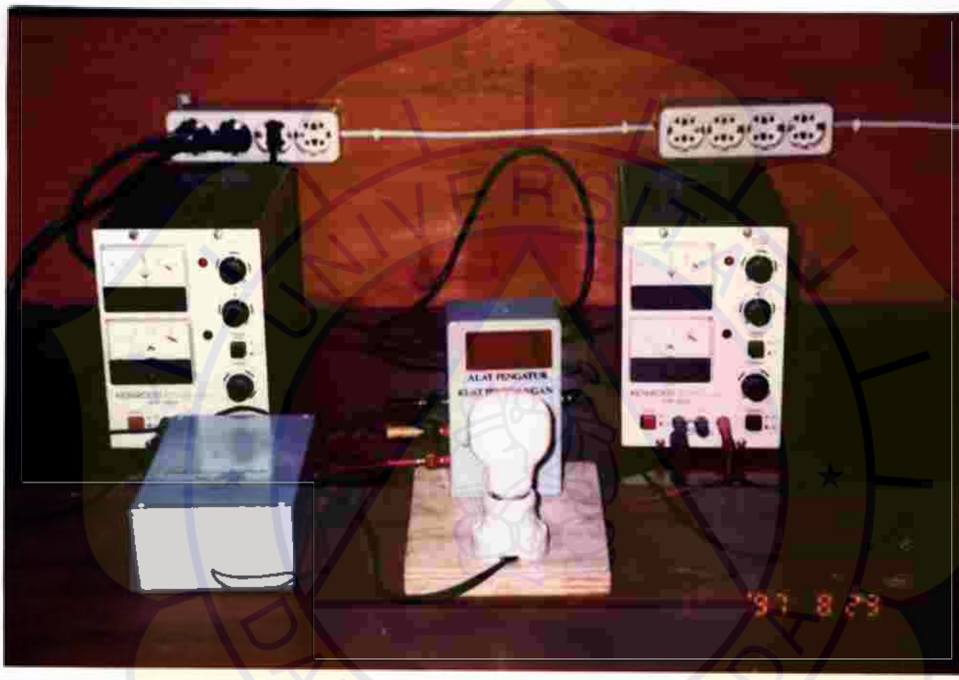
3. Dimensinya relatif cukup kecil, sehingga mudah untuk ditempatkan dimana saja.

4. Untuk mengkalibrasikan alat pengatur yang dibuat cukup mudah, karena dilengkapi dengan pengeset baik pada bagian transduser maupun pada bagian konverter analog ke digital.

DAFTAR PUSTAKA

1. P.vanHarten, *Instaalasi listrik Arus Kuat*, Binacipta, Bandung 1981.
2. Soeharto, *Fisika Dasar II*, PT Gramedia, Jakarta 1992.
3. *301 Rangkaian Elektronika*, PT Elex Media Komputendo Kelompok Gramedia, Jakarta 1995.
4. Warsito S, *Kumpulan Data Penting Komponen*, Multimedia, Jakarta 1986.
5. *Semi-Conductor Application*, Trio-Kenwood Corporation.
6. *New Transistor Manual List*, Electronic Industries Association of Japan.
7. Suharto, *Teknik Sistem dan Kontrol Otomatis*, Djambatan 1985.
8. Richard C Dorf, *Sistem Pengaturan*, Erlangga Jakarta 1983.
9. William D Cooper, Instrumentasi Elektronik dan Teknik Pengukuran, Erlangga Jakarta 1991
10. Francis W Sears, *Optics*, Addisson-Wesley Company, Cambridge Mass 1956.

LAMPIRAN - LAMPIRAN



Gambar Alat Pengatur Kuat Penerangan Digital

LM741/LM741A/LM741C/LM741E operational amplifier

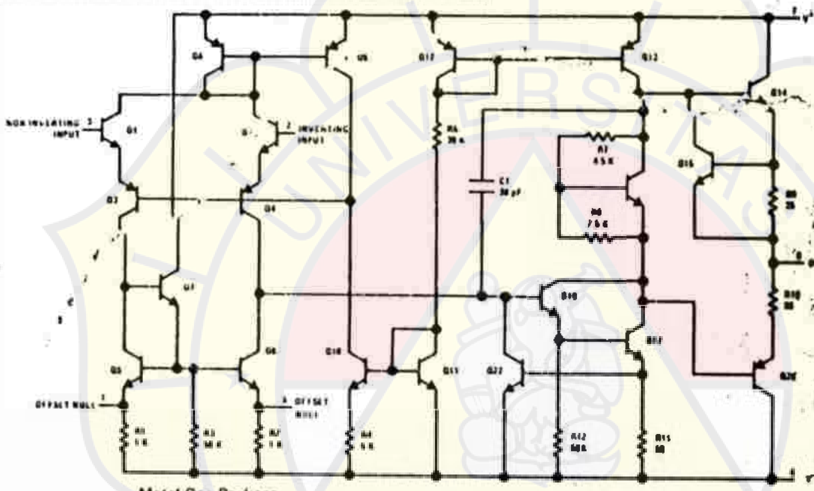
general description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

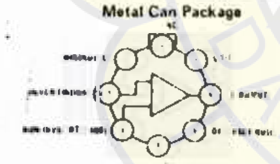
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of -55°C to +125°C.

schematic and connection diagrams (Top Views)



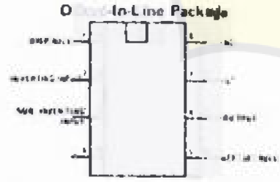
Metal Can Package



Note: Pin 4 connected to case.

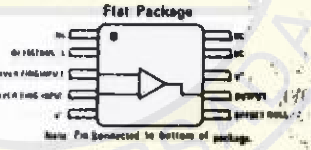
Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package H08C

Dual-In-Line Package



Order Number LM741CN or LM741EN
See NS Package N08B
Order Number LM741CJ or LM741EJ
See NS Package J08A

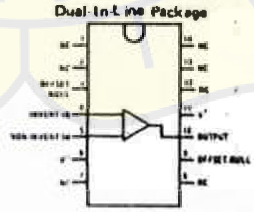
Flat Package



Note: Pin connected to bottom of package.

Order Number LM741F or LM741AF
See NS Package F10A

Dual-In-Line Package



Order Number LM741CD, LM741D, LM741AD or LM741ED
See NS Package D14E
Order Number LM741CN-14
See NS Package N14A
Order Number LM741J-14, LM741AJ-14 LM741CJ-14 or LM741EJ-14
See NS Package J14A

absolute maximum ratings

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Indefinite	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LM741A/LM741E MIN	LM741A/LM741E TYP	LM741A/LM741E MAX	LM741 MIN	LM741 TYP	LM741 MAX	LM741C MIN	LM741C TYP	LM741C MAX	UNITS
Input Offset Voltage	$T_A = 25°C$										
	$R_S \leq 10 k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \leq 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 50\Omega$			4.0							mV
	$R_S \leq 10 k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \leq T_A \leq T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \geq 2 k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2 k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10 k\Omega$	±16									V
	$R_L \geq 2 k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10 k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2 k\Omega$				±10	±13		±10	±13		V

		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.0		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$			150							mW
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: The maximum junction temperature of the LM741/LM741A is 150°C, while that of the LM741C/LM741E is 100°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16 inch thick epoxy glass board with ten, 0.03 inch wide, 2 ounce copper conductors.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time (μs).

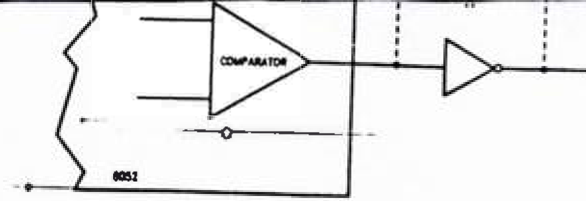


Figure 3

Low Cost Digital Panel Meter Designs

Including Complete Instruction for Intersil's LCD and LED Kits

Intersil's 7106 and 7107 are the first ICs to contain all the active circuitry for a 3½ digit panel meter on a single chip. The 7106 is designed to interface with a liquid crystal display (LCD) while the 7107 is intended for light-emitting diode (LED) displays. In addition to a precision dual slope converter, both circuits contain BCD to seven segment decoders, display drivers, a clock and a reference. To build a high performance panel meter (with auto zero and auto polarity features) it is only necessary to add display, 4 resistors, 4 capacitors, and an input filter if required (Figure 1 and 2).

Note on the ICL7136: The 7136 is an ultra-low-power version of the 7106. Except for the passive component values as shown in Figure 3 and Table 1, all references in this document to the ICL7106 also apply to the ICL7136.

COST ADVANTAGES OF 7106 AND 7107

Until recently, the make or buy decision for any A-to-D system was dominated by the engineering costs. Even a simple panel meter, built from off-the-shelf digital and linear ICs, required at least six months of engineering effort for completion. However, the advent of truly single chip panel meter functions (Intersil's 7106 and 7107) has reduced the design effort on the part of the user to zero. The make or buy decision becomes a simple question of dollars and cents.

At the time of writing (1982), a 3½ digit LED display panel meter can be built for $18 in production (5,000) quantities. This figure includes labor at $3 per hour with 300% overhead. The cost breakdown is as follows:

(Prices are subject to change)

ICL7107 (@5000 pcs)	$5.95
LEDs (4)	3.00
Capacitors (5)	58
Resistors (4)	12
Potentiometer	60
Circuit Board	1.00
Misc Hardware	75
TOTAL COMPONENTS	$12.00
Labor (½ hour at $3/hour, 300% overhead)	6.00
TOTAL COST including assembly and test	$18.00

A 3½ digit LCD panel meter, using the 7106, is $3 to $4 more expensive. This is due to the greater cost of the display.

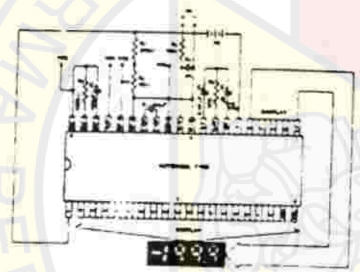


Figure 1: LCD Digital Panel Meter Using ICL7106

Figure 2: LED Digital Panel Meter Using ICL7107

These cost figures are considerably lower than the cost expensive of the ready-built panel meters. However, the cost is not the only advantage; the do-it-yourself approach allows greater flexibility. Off-the-shelf panel meters have form factors which are frequently inconvenient, whereas a single IC design takes up a minimum of circuit board real estate. Consider the advantages for field servicing a military radar, for example, if each complex circuit card had its own built-in voltmeter and miniature switch. Fault finding would be greatly simplified by making critical voltages throughout the system instantly accessible.

THE EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½ digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

Assembly Instructions

The circuit board layouts and assembly drawings for both kits are given in the Appendices. The boards are single-sided to minimize cost and simplify assembly. Jumpers are used to allow maximum flexibility. For example, provision has been made for connecting an external clock (Test Point #5). Provision has also been made for separating REF Lo from COMMON when using an external reference zener. In a production instrument, the board area could be reduced dramatically. Aside from the display, all the components can easily be placed in less than 4 square inches of board space.

- Molex* pins are used to provide a low cost IC socket; one circuit board can thus be used to evaluate several ICs. (Strips of 20 pins should be soldered onto the P.C. boards, the top of the strip holding the pins together can then be broken off by bending it back and forth using needle-nose pliers). Solder terminals are provided for the five test points, and for the ±5V input on the 7107 kit.

Full Scale Reading - 200mV or 2.000V?

The component values supplied with the kit are those specified in the schematics of Figure 1 or Figure 2. They have been optimized for 200.0mV full scale reading. The complete absence of last digit jitter on this range illustrates the exceptional noise performance of the 7106 and 7107. In fact, the noise level (not exceeded 95% of time) is about 15μV, a factor of 10 less than some competitive one chip panel meters.

To modify the sensitivity of 2.000 volts full scale, the integrator time constant and the reference should be changed by substituting the component values given in the Table below. The auto-zero capacitor (C_2) should also be changed. These additional components are not supplied in the kits. In addition, the decimal point jumper should be changed so the display reads 2.000.

Table 1: Component Values for Full Scale Options

Component (type)	200.0 mV Full Scale	2.000 V Full Scale
C_2 (mylar)	0.47 μF	.047 μF
R_1	24 kΩ	1.5 kΩ*
R_2	47 kΩ	470 kΩ
C2	0.1 μF	0.022 μF
R1	220 kΩ	150 kΩ
R2	180 kΩ	1.8 MΩ
R4	10 kΩ	100 kΩ

* Changing R_1 to 1.5kΩ will reduce the battery life of the 7106 kit. As an alternative, the potentiometer can be changed to 25kΩ.

Liquid Crystal Display (7106)

Liquid crystal displays are generally driven by applying a symmetrical square wave to the back-plan (B.P.). To turn on a segment, a waveform 180° out of phase with B.P. (but of equal amplitude) is applied to that segment. Note that excessive D.C. voltages (>50mV) will permanently damage the display if applied for more than a few minutes. The 7106 generates the segment drive waveform internally, but the user should generate the decimal point front plane drive by inverting the B.P. (pin 21) output.** In applications where the decimal point remains fixed, a simple MOS inverter can be used (Figure 4). For instruments where the decimal point** must be shifted, a quad exclusive OR gate is recommended (Figure 5). Note that in both instances, TEST (pin 37, TP1) is used as V− for the inverters. This pin is capable of sinking about 1mA, and is approximately 5 volts below V+. The B.P. output (pin 21) oscillates between V+ & TEST

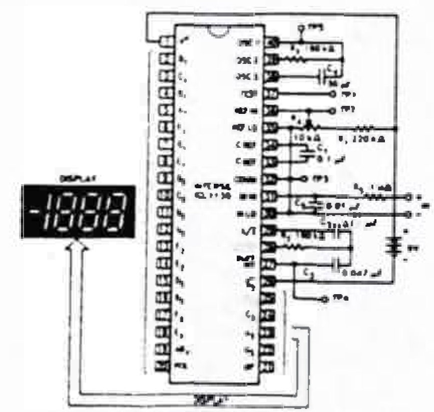


Figure 3: LCD Digital Panel Meter Using ICL7136

the decimal point pad to COMMON [illegible] at about 2.8 volts below V+. Prolonged use of this technique, however, may permanently burn-in the decimal because COMMON is not exactly midway between B.P. high and B.P. low.

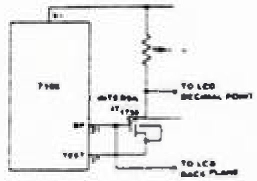


Figure 4: Simple Inverter for Fixed Decimal Point

Before soldering the display onto the circuit board, make sure that it is inserted correctly. Many LCD packages do not have pin #1 marked, but the segments of an unenergized display can be seen by viewing with reflected light. The package orientation should correspond with that shown in Appendix I.

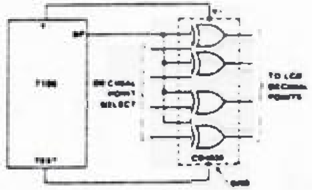


Figure 5: Exclusive 'OR' Gate for Decimal Point Drive

Light Emitting Diode Display (7107)

The 7107 pull-down FETs will sink about 8mA per segment. Using standard common anode 0.3" or 0.43" red LEDs, this drive level produces a bright display suitable for almost any indoor application. However, additional brightness can be achieved through the use of Hewlett Packard high-efficiency LEDs. Note that the display contrast can be increased substantially by using a filter. Ref. 4 discusses filter techniques and lists manufacturers of suitable materials.

A fixed decimal point can be turned on by tying the appropriate cathode to ground through a 150Ω resistor. The circuit boards [illegible] with the [illegible] accommodate either [illegible] the popular 3700 types. The difference [illegible] displays or two is that [illegible] MAN 3700 uses pin 9 [illegible] the decimal point [illegible] between the 6, whereas the [illegible] decimal point, catode on pin [illegible] on the circuit board [illegible] points are wired [illegible] jumper pads; it may be directly brought to 150Ω resistor to the display. For multiple range [illegible], a 7400 series CMOS quad gate or buffer should [illegible] from the [illegible]. The majority of them are capable of sinking about [illegible] 8mA [illegible] should be used.

Capacitors

The integrator capacitor should be a low dielectric-loss type. Long term stability and temperature coefficient are unimportant since the dual slope technique cancels the effect of these. [illegible] polypropylene capacitors have been found to work well; they have low dielectric loss characteristics and are [illegible] suitable [illegible]. That is not to say that they are the only types [illegible] capacitors are satisfactory for C_1 (reference) and C_2 (auto-zero).

For a more detailed discussion of recommended capacitor types, the reader is referred to page 3 of Reference 2.

A simple RC oscillator is used in the kit. It runs at about 48kHz and is divided by 4 prior to being used as the system clock (Figure 6). The internal clock period is thus 83.3µs, and the signal integration period (1000 clock pulses) is 83.3 mS. The measurement sequence requires 4000 clock pulses per measurement, giving 3 readings per second. Setting the clock oscillator at precisely 48kHz will result in optimum line frequency (60Hz) noise rejection, since the integration period is an integral number of line frequency periods (see Ref. 2 for discussion). Countries with 50Hz line frequencies should set the clock at 50kHz.

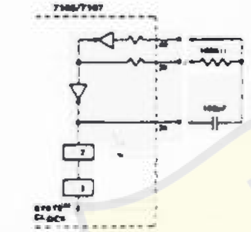


Figure 6: 7106/7107 Internal Oscillator/Clock

An external clock can also be used. In the 7106, the internal logic is referenced to TEST. External clock waveforms should therefore swing between TEST and V+ (Figure 7a). In the 7107, the internal logic is referenced to GND so any generator whose output swings from ground to +5V will work well (Figure 7b).

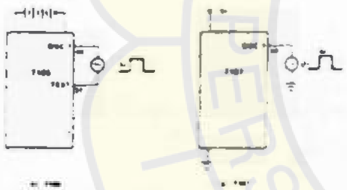


Figure 7: External Clock Options

The Reference

For 200.0mV full scale, the voltage applied between REF Hi and REF Lo should be set at 100.0mV. For 2.000V full scale, set the reference voltage at 1.000V. The reference inputs are floating, and the only restriction on the applied voltage is that it should lie in the range V- to V+.

The voltage between V+ and COMMON is internally regulated at about 2.8 volts. This reference is adequate for many applications and is used in the evaluation kits. It has a typical temperature coefficient of 100ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance due to its higher thermal resistance. [illegible] ceramic [illegible] plastic parts [illegible] more [illegible] this respect than the ceramic. The performance is cautioned against extrapolating from the performance of the 7107 supplied with a ceramic package to a plastic part. The combination of reference TC, internal chip dissipation, and package thermal resistance can increase noise near full scale from 25µV to 80µV pk-pk.

as 1111 (6 segments on) can also suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a nonoverload count as the die alternately heats and cools. These problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added as shown in Figures 8(a) or 8(b).

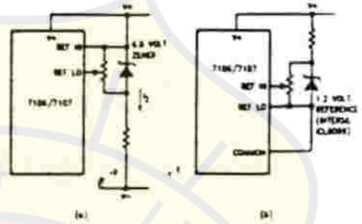


Figure 8: Using an External Reference

Power Supplies

The 7106 kit is intended to be operated from a 9 volt dry cell. INPUT Lo is shorted to COMMON, causing V+ to sit 2.8 volts positive with respect to INPUT Lo, and V- 6.2 volts negative with respect to INPUT Lo.

The 7107 kit should be operated from ±5 volts. Noisy supplies should be bypassed with 6.8µF capacitors to ground at the point where the supplies enter the board. INPUT Lo has an effective common mode range with respect to GND of a couple of volts.

The precise value is determined by the point at which the integrator output ramps within ~.3V of one or other of the supply rails. This is governed by the integrator time constant, the magnitude and polarity of the input, the common mode voltage, and the clock frequency; for further details, consult the data sheet. Where the voltage being measured is floating with respect to the supplies, INPUT Lo should be tied to some voltage within the common mode range such as GROUND or COMMON. If a -5 volt supply is unavailable, a suitable negative rail can be generated locally using the circuit shown in Figure 9.

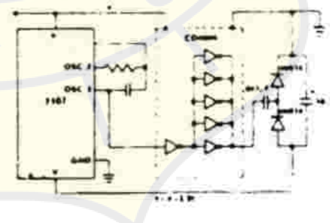


Figure 9: Generating Negative Supply From +5V

extremely low input leakage current, typically 1pA at 25°C. This minimizes the errors caused by high impedance passive filters on the input. For example, the simple RC (1MΩ/.01µF) combination used in the evaluation kits introduces a negligible 1µV error.

PRELIMINARY TESTS

Auto Zero

With power on and the inputs shorted, the display should read zero. The negative sign should be displayed about 50% of the time, an indication of the effectiveness of the auto-zero system used in the 7106 and 7107. Note that some competitive circuits flash negative on every alternate conversion for inputs near zero. While this may look good to the uninitiated, it is not a true auto zero system!

Over-range

Inputs greater than full scale will cause suppression of the three least significant digits, i.e. only 1 or -1 will be displayed.

Polarity

The absence of a polarity signal indicates a positive reading. A negative reading is indicated by a negative sign.

Further evaluation should be performed with the help of a precision DC voltage calibrator such as Fluke Model 343A. Alternatively a high quality 4½ digit DVM can be used, provided its performance has been measured against that of a reliable standard.

CAUTION: Potential trouble areas when constructing the evaluation kits.

1. **Certain LCD displays have a protective plastic sheet covering the plastic top. This sheet may be removed after installing the display to maximize display viewing.**
2. **Solder flux or other impurities on PC board may cause leakage paths between IC pins and board traces reducing performance and should be removed with rubbing alcohol or some other suitable cleaning agent. Displays should be removed when cleaning as damage could result to them.**
3. **Blue PC board material (PC75) has been treated with a chemical which may cause surface leakage between the input traces. It is suggested that the board be scribed between the input traces and adjacent traces to eliminate this surface leakage.**
4. **In order to ensure that unused segments on the LCD displays do not turn on, tie them to the backplane pin (pin 21).**

[Purpose]

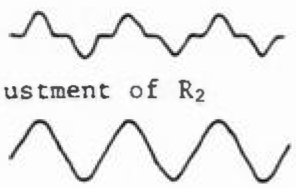
This is to understand functional principles of single end push-pull amplification of NPN and PNP transistors without phase reverse circuit.

[Measuring Equipment]

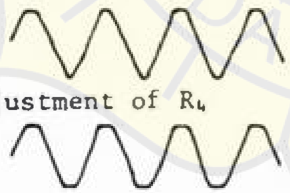
Low frequency oscillator ... 1 pc.
Oscilloscope ... 1 pc. A.C. voltmeter ... 1 pc.

[Experiment Steps]

1. Arrange blocks as shown in the block diagram and make sure that there is no misarrangement.
2. By the use of terminal cords, link each measuring instruments and the power supply which should be adjusted to 12V.
3. Adjust attenuator in the oscillator by increasing it gradually so that no distorted output waves may be produced at the maximum output power.
4. Wave distortion can be adjusted by variable resistance R_3 and R_L. Then turn up the oscillator so that both upper and lower wave forms may be clipped at the same time as shown in the figure 1.
5. Check output and input characteristics as well as frequency characteristic and make a graph of them.



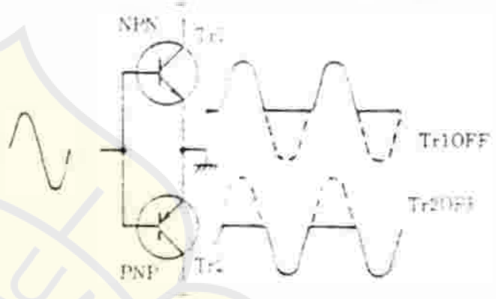
Adjustment of R_2

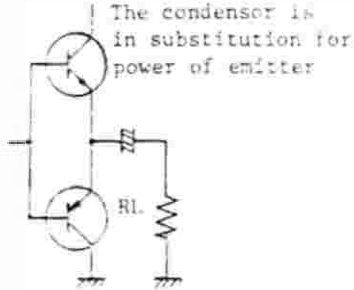


Adjustment of R_4

[Reference]

In the circuit in which NPN and PNP transistor bases are tive against the emitter and it turns off when the base is negative. PNP, however, functions when the base is negative and turns off when the base is positive. NPN and PNP transistors alternately function at every positive and negative half cycle. In other words, without phase reverse circuit, transistors can function by turns.





(C_1: maintenance condenser)
Without this condenser, base currency decreases and output power gets lower as base voltage of Tr2 increases when Tr1 collector voltage increases and Tr2 has a positive half cycle. If you add C_1, Tr1 collector voltage will go up and Tr2 collector currency will increase as well as the emitter voltage. Since C_1 voltage does not alter suddenly, the point (1) voltage goes up, and R_2 currency maintai[illegible]. Therefore, Tr2 base currency is ensured. R_L gives R.C. negative feedback to Tr1. This prevents Tr1 from altering the output voltage due to the temperature changes.

[General Wiring Diagram]