BAB V

KESIMPULAN

Dari uraian bab-bab terdahulu dan dari hasil pengamatan, maka dapat ditarik beberapa kesimpulan, yaitu :

1. Dalam sistem proteksi kendaraan bermotor ini mempunyai keuntungan yaitu, dapat memberi informasi kepada pemiliknya melalui penerima yang dipancarkan oleh pemancar dari kendaraan selama alarm belum dimatikan.
2. Dengan kunci koding digital dapat memberi keamanan dan kemudahan bagi pemakainya, karena kombinasi dari kunci dapat ditentukan sesuai keinginan.
3. Alat proteksi ini sangat fleksibel dapat digunakan juga pada proteksi rumah, gudang dan sebagaimya, yaitu dengan menghilangkan kapasitor C_1 dan eksternal sakelar sebagai sensornya.

DAFTAR PUSTAKA

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   "Security Electronics" third Edition

2. HELMS HARRY. L

   "Electronics Applications" source book one Edition, 1980

3. 302, 303 CIRCUITS

   Penerbit PT. Elex Media Komputindo, Kelompok-Gramedia, Jakarta

4. MILLMAN JACOB Ph. D, SUTANTO

   "Mikro Elektronika Sistem Digital dan Rangkaian-Analog", Jilid 1 dan 2, Penerbit Erlangga, 1986

5. BARMAWI MALVINO,

   "Prinsip-prinsip Elektronika", Edisi ketiga,-Jilid 1, Penerbit Erlangga, 1986

LAMPIRAN-LAMPIRAN

BD 135 · BD 137 · BD 139

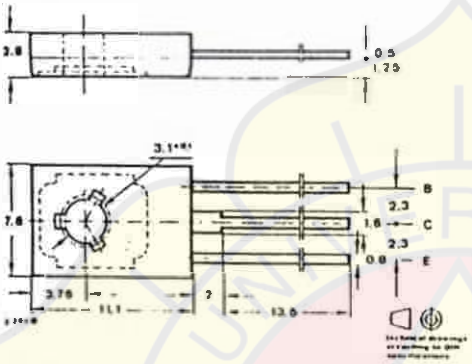
Silicon NPN Epitaxial Planar Power Transistors

Applications: General in AF-range

Features:

- Power dissipation 8 W
- Matched pairs available
- BD 135, BD 136, BD 139 are complementary to BD 136, BD 138, BD 140

Dimensions in mm



Collector connected with metallic surface

Case
12 A 3 DIN 41869
JEDEC TO 126 (SOT 32)
Weight max. 0.8 g

Accessories

Isolating washer Best. Nr. 119880
Washer 3.2 DIN 125A

Absolute maximum ratings		BD 135	BD 137	BD 139	
Collector-base voltage	V_{CBO}	45	60	80	V
Collector-emitter voltage	V_{CEO}	45	60	80	V
Emitter-base voltage	V_{EBO}		5		V
Collector current	I_C		1		mA
Collector peak current	I_{CM}		1,5		A
Base current	I_B		100		mA
Total power dissipation					
$T_{amb} \leq 45°C$	P_{tot}		1		W
$T_{case} \leq 70°C$	P_{tot}		8		W
Junction temperature	T_j		150		°C
Storage temperature range	T_{stg}		−55...+150		°C
Tightening torque	M_A [1]		70		Ncm

[1] with screw M 3 and washer 3.2 DIN 125 A

TI.2/502.0484E)

BD 135 · BD 137 · BD 139

			Min.	Typ.	Max.	
Thermal resistances						
Junction ambient		R_{thJA}			100	K/W
Junction case		R_{thJC}			10	K/W
Characteristics						
T_{amb} = 25 °C, unless otherwise specified						
Collector cut-off current						
V_{CB} = 30 V		I_{CBO}			100	nA
V_{CB} = 30 V, T_{amb} = 150 °C		I_{CBO}			100	µA
Collector-base breakdown voltage						
I_C = 1 mA	BD 135	$V_{(BR)CBO}$	45			V
	BD 137	$V_{(BR)CBO}$	60			V
	BD 139	$V_{(BR)CBO}$	80			V
Collector-emitter breakdown voltage						
I_C = 2.0 mA	BD 135	$V_{(BR)CEO}$ [1]	45			V
	BD 137	$V_{(BR)CEO}$ [1]	60			V
	BD 139	$V_{(BR)CEO}$ [1]	80			V
Emitter-base breakdown voltage						
I_E = 1 µA		$V_{(BR)EBO}$	5			V
Collector saturation voltage						
I_C = 500 mA, I_B = 50 mA		V_{CEsat} [1]			500	mV
Base-emitter voltage						
V_{CE} = 2 V, I_C = 500 mA		V_{BE} [1]			1	mV
DC forward current transfer ratio						
V_{CE} = 2 V, I_C = 150 mA	BD 135	h_{FE} [1]	40		250	
	BD 137, BD 139	h_{FE} [1]	40		160	
V_{CE} = 2 V, I_C = 500 mA		h_{FE} [1]	25			
h_{FE} matched pair ratio						
V_{CE} = 2 V, I_C = 150 mA [1]					1.4	
Gain bandwidth product						
V_{CE} = 5 V, I_C 50 mA, f = 30 MHz		f_T	50			MHz

[1] $\frac{t_p}{T}$ = 0.01, t_p = 0.3 ms

Typ Type Type Tipo	Hersteller Manufacturers Fabricants Produttori	M/Pol. M/Pol. M/Pol. M/Pol.	Bild Fig. Fig. Fig.	Kurzbeschreibung Short description Description succ. Descrizione somm.	Vergleichstypen (Bild) Comparison types (fig.) Types d'equivalence (fig.) Tipi correspondenti (fig.)	Anmerkungen Notes Notes Note
BC 210 BC 211	SGS SGS	Si-NPN Si-PNP	6 6	NF-Tr/E, 30V, 1A, 0,8W NF-Tr/E, 30 V, 1A, 0,8W	BC 141 (6), BC 301 (6), BC 341 (6) BC 161 (6), BC 303 (6), BC 361 (6)	kompl.: BC 211 kompl.: BC 210
BC 212	SGS	Si-NPN	6	NF, 100 V, 0,15A, 0,8W	BC 141 (6), BC 301 (6), BF 257 (6), BF 336 (6)	
BC 213 (-6...-16) (A...6) BC 213 A	MIS, SES " SES	Si-PNP " Si-PNP	6 " 6	NF-Tr/E, 60V, 1A, 0,8W " = BC 213, 80V	BC 161 (6), BC 304 (6), BC 461 (6) BC 303 (6), BC 461 (6)	kompl.: BC 211 kompl.: BC 211 A
BC 214	SGS	Si-NPN	4	Uni, 1 20V, 0 ,830,1W w	BC 285 (4a), BC 236 (4), BC 532 (21a), BF 297 (21a), BF 422 (21)	
BC 215 (-6...-16)	TIX	Si-PNP	21a	NF-V-w, 45 V, 0,1A, 0,3W	BC 212 (21a), BC 415 (21a), BC 560 (21a)	
BC 317 (A, B) BC 318 (A, B, C) BC 319 (B, C)	MOT MOT MOT	Si-NPN Si-NPN Si-NPN	21a 21a 21a	Uni, 50 V, 0,15A, 0,35W 280MHz, B=125-500 Uni, 40V, 0,15A, 0,35W 280MHz, B=125-900 Uni-w, 30 V, 0,15A, 0,35W 280MHz, B=240-900	BC 107 (4a), BC 171 (21a), BC 182 (21a), BC 207 (4), BC 237 (21a), BC 382 (21a), BC 547 (21a), BC 582 (21a) kompl.: BC 320 BC 107 (4a), BC 171 (21a), BC 183 (21a), BC 207 (4), BC 237 (21a), BC 382 (21a), BC 547 (21a), BC 582 (21a) kompl.: BC 321 BC 108 (4a), BC 173 (21a), BC 184 (21a), BC 108 (4), BC 239 (21a), BC 384 (21a), BC 549 (21a), BC 584 (21a) kompl.: BC 322
BC 320 (A, B) BC 321 (A, B, C) BC 322 (B, C)	MOT MOT MOT	Si-PNP Si-PNP Si-PNP	21a 21a 21a	Uni 50V, 0,15A, 0,31W 250MHz, B=125-500 Uni 45V, 0,15A, 0,31W 250MHz, B=125-900 Uni-w, 30V, 0,05A, 0,31W 250MHz, B=240-900	BC 177 (4a), BC 204 (4), BC 212 (21a), BC 251 (21a), BC 307 (21a), BC 512 (21a), BC 557 (21a) kompl.: BC 317 BC 177 (4a), BC 204 (4), BC 213 (21a), BC 251 (21a), BC 307 (21a), BC 512 (21a), BC 557 (21a) kompl.: BC 318 BC 179 (4a), BC 206 (4), BC 214 (21a), BC 253 (21a), BC 309 (21a), BC 514 (21a), BC 559 (21a) kompl.: BC 319
BC 323	SGS	Si-NPN	6	TV-VA, 100V, 5A, 0,8W	2N5338, 39 (6)	
BC 324	SGS	Si-NPN	6	TV -VA, 80V, 1A, 0,8W	BC 141 (6), BC 301 (6)	
BC 325 BC 326	TIX TIX	Si-PNP Si-PNP	4a 4a	NF-w, 60V, 0,05A, B>40 NF-w, 80V, 0,05A, B>100	BC 212 (21a), BC 416 (21a), BC 560 (21a), BC 526 (21a) BC 212 (21a), BC 416 (21a), BC 560 (21a), BC 526 (21a)	
BC 327 (-16...-40) BC 327-01	AEG, ITT, MUL, PHI, SES, SGS, SIE, TIX, VAL ELC	Si-PNP Si-PNP	21a 20	NF-Tr, 50V, 0,8A, 0,625W = BC 327, 0,5 A, 0,4W	BC 297 (4a), BC 727 (21a), BC 827 (21a) kompl.: BC 337 BC 636 (21)	
BC 328 (-16...-40) BC 328-01	AEG, ITT, MUL, PHI, SES, SGS, SIE, TIX, VAL ELC	Si-PNP Si-PNP	21a 20	NF-Tr, 30V, 0,8A, 0,625W = BC 328, 0,5A, 0,4W	BC 298 (4a), BC 728 (21a), BC 828 (21a) kompl.: BC 338 BC 636 (21)	

Typ Type Type Tipo	Hersteller Manufacturers Fabricants Produttori	M/Pol. M/Pol. M/Pol. M/Pol.	Bild Fig. Fig. Fig.	Kurzbeschreibung Short description Description succ. Descrizione somm.	Vergleichstypen (Bild) Comparison types (fig.) Types d'equivalence (fig.) Tipi correspondenti (fig.)	Anmerkungen Notes Notes Note
BC 329 (B, C) BC 330 (B, C) BC 331 (A, B, C) BC 332 (A, B, C)	TIX TIX TIX TIX	Si-NPN Si-NPN Si-NPN Si-NPN	21a 21a 21a 21a	NF-s-w, 60 V, 0,03A, 0,25 W NF-s-w, 45 V, 0,03A, 0,25 W NF-w, 60V, 0,03A, 0,25W NF-w, 45V, 0,03A, 0,25W	BC 414 (21a), BC 520 (21a), BC 550 (21a) BC 414 (21a), BC 521 (21a), BC 550 (21a) BC 414 (21a), BC 520 (21a), BC 550 (21a) BC 414 (21a), BC 521 (21a), BC 550 (21a)	
BC 333 BC 334 BC 335 BC 336	MOT MOT MOT MOT	Si-NPN Si-PNP Si-NPN Si-PNP	21a 21a 21a 21a	Uni 25 V, 0,05A, 0,31W >50MHz, B=100-1000 Uni 25 V, 0,05A, 0,31W >50MHz, B=100-1000 Uni-s 25 V, 0,05A, 0,31W >50MHz, B=100-1000 Uni-s, 25 V, 0,05A, 0,31W >50MHz, B=100-1000	BC 108 (4a), BC 172 (21a), BC 182 (21a), BC 208 (4), BC 238 (21a), BC 383 (21a), BC 547 (21a), BC 583 (21a) kompl.: BC 334 BC 178 (4a), BC 205 (4), BC 213 (21a), BC 252 (21a), BC 308 (21a), BC 512 (21a), BC 558 (21a) kompl.: BC 333 BC 108 (4a), BC 173 (21a), BC 184 (21a), BC 208 (4), BC 239 (21a), BC 384 (21a), BC 549 (21a), BC 584 (21a) kompl.: BC 336 BC 179 (4a), BC 206 (4), BC 214 (21a), BC 253 (21a), BC 309 (21a), BC 514 (21a), BC 559 (21a) kompl.: BC 335
BC 337 (-16/40) BC 337-01	AEG, ITT, MUL, PHI, SES, SGS, SIE, TIX, VAL ELC	Si-NPN Si-NPN	21a 20	NF-Tr, 50V, 0,8A, 0,625W = BC 337, 0,5A, 0,4W	BC 377 (4a), BC 737 (21a), BC 837 (21a) kompl.: BC 327 BC 637 (21)	
BC 338 (-16...-40) BC 338-01	AEG, ITT, MUL, PHI, SES, SGS, SIE, TIX, VAL ELC	Si-NPN Si-NPN	21a 20	NF-Tr, 30V, 0,8A, 0,625 W = BC 338, 0,5A, 0,4W	BC 378 (4a), BC 738 (21a), BC 838 (21a) kompl.: BC 328 BC 635 (21)	
BC 340 (-6...-16) BC 341 (-6...-16)	ITT ITT	Si-NPN Si-NPN	4a 6	NF-Tr/E, 60 V, 0,5A, 0,6W NF-Tr/E 60 V, 0,5A, 0,6W	BC 140 (6), BC 302 (6) BC 140 (6), BC 301 (6)	kompl.: BC 360 kompl.: BC 361
BC 342 BC 343 BC 344 BC 345	MOT MOT MOT MOT	Si-NPN Si-PNP Si-NPN Si-PNP	6 6 6 6	NF-Tr/E, 70 V, 1A, 0,8W NF-Tr/E, 70 V, 1A, 0,8W NF-Tr/E 90V, 1A, 0,8W NF-Tr/E, 90 V, 1A, 0,8W	BC 141 (6), BC 301 (6) BC 161 (6), BC 303 (6) BC 141 (6), BC 301 (6) BC 303 (6)	kompl.: BC 343 kompl.: BC 342 kompl.: BC 345 kompl.: BC 344
BC 347 (A, B, L) BC 348 (A, B, L) BC 349 (A, B, L)	MOT MOT MOT	Si-NPN Si-NPN Si-NPN	21a 21a 21a	Uni, 50 V, 0,1A, 0,3W >125MHz, B=40-450 Uni, 40 V, 0,1A, 0,3W >125MHz, B=40-450 Uni, 30 V, 0,1A, 0,3W >125MHz, B=40-450	BC 107 (4a), BC 171 (21a), BC 182 (21a), BC 207 (4), BC 237 (21a), BC 382 (21a), BC 547 (21a), BC 582 (21a) kompl.: BC 350 BC 107 (4a), BC 171 (21a), BC 183 (21a), BC 207 (4), BC 237 (21a), BC 382 (21a), BC 547 (21a), BC 582 (21a) kompl.: BC 351 BC 108 (4a), BC 172 (21a), BC 183 (21a), BC 208 (4), BC 238 (21a), BC 383 (21a), BC 548 (21a), BC 583 (21a) kompl.: BC 352
BC 350 (A, B, L) BC 351 (A, B, L)	MOT MOT	Si-PNP Si-PNP	21a 21a	Uni, 50V, 0,1A, 0,3W >125MHz, B=40-450 Uni, 40V, 0,1A, 0,3W >125MHz, B=40-450	BC 177 (4a), BC 204 (4), BC 212 (21a), BC 251 (21a), BC 307 (21a), BC 512 (21a), BC 557 (21a) kompl.: BC 347 BC 178 (4a), BC 204 (4), BC 213 (21a), BC 251 (21a), BC 307 (21a), BC 512 (21a), BC 557 (21a) kompl.: BC 348	

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BC480(-6, -10) (A, B, L)	MOT	Si-PNP	21e	NF-Tr/E, 60V, 1A, 0,625W	BC527 (21e), BC534 (21e) BC638 (21)	kompl.: BC487
BC489(-6, -10) (A, B, L)	MOT	Si-NPN	21e	NF-Tr/E, 80V, 1A, 0,625W	BC535 (21e), BC538 (21e) BC639 (21)	kompl.: BC490
BC490(-6, -10) (A, B, L)	MOT	Si-PNP	21e	NF-Tr/E, 80V, 1A, 0,625W	BC534 (21e), BC538 (21e) BC640 (21)	kompl.: BC489
BC 507 (F) (A, B)	SGS	Si-NPN	21e	Uni, 30V, 0,2A, 0,36W 200MH I_C=1 0-4 50	BC 174 (21e), BC 190 (4a), BC546 (21e)	
BC 508 (F) (A, B, C)	SGS	Si-NPN	21e	Uni, 60V, 0,2A, 0,36W 200MH$_{z}$ -6 1 0-4 50	BC 174 (21e), BC 182 (21e), BC 190 (4a), BC546 (21e)	
BC 509 (F) (B, C)	SGS	Si-NPN	21e	Uni-re, 60V, 0,2A, 0,36W 200MHz, B=200-450	BC 184 (21e), BC 384 (21e), BC 414 (21e), BC 550 (21e)	
BC 510 (F) (B, C)	SGS	Si-NPN	21e	Uni-re, 40V, 0,2A, 0,36 W 300MHz, 4200 -4 60	BC 184 (21e), BC 384 (2a), BC 413 (21e), BC 550 (21e)	
BC 512 (A, B,)	TIX	Si-PNP	21e	Uni, 50V, 0,2A, 0,3W >200MHz, B=100-480	BC 177 (4a), BC 204 (4), BC 2 1 2(2a) , BC 251 (21e), BC307 (21e), BC 557 (21e)	kompl.: BC 52 2
BC 513 (A, B, C)	TIX	Si-PNP	21e	Uni, 30V, 0,2A, 0,3W >200MHz, B=100-600	BC 178 (4a), BC 205 (4), BC 213 (21e), BC 558 (21e)	BC 252 (21e), BC 308 (21e), kompl.: BC 543
BC 514 (A, B, C)	TIX	Si-PNP	21e	Uni-re, 30V, 0,2A, 0,3W >200MHz, B= 100-600	BC 178 (4a), BC 206 (4), BC 214 (21e), BC 559 (21e)	BC 253 (21e), BC 309 (21e), kompl.: BC 544
BC 516	TIX	Si-PNP	21e	Darl, 40V, 0,4A, 0,625W	BC 876 (21), MPS-A65-66 (21e)	kompl.: BC 517
BC 517	TIX	Si-NPN	21e	Darl, 40V, 0,4A, 0,625W	BC 875 (21), MPS-A13-14 (21e)	kompl.: BC 516
BC 520 (B, C)	FCH	Si-NPN	21e	Uni-re, 60V, 0,05A, 0,625W B=180-800	BC 329 (21e), BC 414 (21e), BC560 (21e)	
BC 521 (C, D)	FCH	Si-NPN	21e	Uni-re, 45V, 0,05A, 0,625W B=380-1550	BC 330 (21e), BC 384 (21e), BC 413 (21e), BC550 (21e)	
BC 522 (C, D, E)	FCH	Si-NPN	21e	Uni-re, 20V, 0,05A, 0,625W B=380-2200	BC 330 (21e), BC 384 (21e), BC 413 (2a), BC 549 (21e)	
BC 523 (B, C)	FCH	Si-NPN	21e	Uni-re, 45V, 0,05A, 0,625W B=180-800	BC 330 (21e), BC 384 (2a), BC 414 (21e), BC 550 (21e)	
BC 524 (B, C)	TIX	Si-NPN	21e	Uni 45V, 0,1A, 0,625W	BC 547 (21e)	
BC 526	FCH	Si-PNP	21e	Uni-re, 45V, 0,1A, 0,625W B=100-300	BC 560 (21e)	
BC 526 (A, B, C)	FCH	Si-PNP	21e	Uni-re, 60V, 0,2A, 0,625W	BC 560 (21e)	

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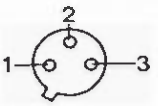
BC 527 (6...-25)	FCH	Si-PNP	21e	NF-Tr/E, 60V, 1A, 0,625W	BC 534 (21e), BC 488 (21e) BC 638 (21)	kompl.: BC 537
BC 528 (6...-25)	FCH	Si-PNP	21e	NF-Tr/E, 80V, 1A, 0,625W	BC 534 (21e), BC 490 (21e) BC 640 (21)	kompl.: BC 538
BC 529	FCH	Si-PNP	21e	Uni, 50V, 0,2A, 0,625W >100MHz, B=60-300	BC 557 (21e)	
BC 530	FCH	Si-NPN	21e	Vid, 30V, 0,1A, 0,625W >50MH$_{z}$ B=40-180	BF 398 (21e), 2N3930-31 (4a) BF 423 (21)	kompl.: BC 532
BC 531	FCH	Si-PNP	21e	Vid, 60V, 0,1A, 0,625W >50MHz B=60-240	BF 396 (21e), 2N3930-31 (4a) BF 423 (21)	kompl.: BC 533
BC 532	FCH	Si-NPN	21e	Vid, 60V, 0,1A, 0,625W >50MHz, B=60-250	BF 297 (21e), 2N5550 (21e) BF 422 (21)	kompl.: BC 530
BC 533	FCH	Si-NPN	21e	Vid, 180V, 0,1A, 0,625W >50MHz, B=40-250	BF 298 (2a), 2N5551 (21e) BF 422 (21)	kompl.: BC 531
BC 534	FCH	Si-PNP	21e	NF-Tr/E, 80V, 0,5A, 0,625W	BC 490 (2a), BC 528 (21e) BC 640 (21)	kompl.: BC 535
BC 535	FCH	Si-NPN	21e	NF-Tr/E, 80V, 0,5A, 0,625W	BC 489 (2a), BC 538 (21e) BC 639 (21)	kompl.: BC 534
BC 537 (6...-25)	FCH	Si-NPN	21e	NF-Tr/E, 60V, 1A, 0,625W	BC 535 (21e), BC 487 (21e) BC 638 (21)	kompl.: BC 527
BC 538 (6...-25)	FCH	Si-NPN	21e	NF-Tr/E, 80V, 1A, 0,625W	BC 535 (21e), BC 489 (21e) BC 639 (21)	kompl.: BC 528
BC 546 (V, A, B)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni 80V, 0,2A, 0,5W 300MH$_{z}$ B=180-800	BC 174 (21e), BC 190 (4a), BC 447 (21e)	kompl.: BC 556
BC 547 (V, A, B, C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni, 50V, 0,2A, 0,5W 300MHz, B=75-800	BC 107 (4a), BC 171 (21e), BC 182 (21e), BC 207 (4), BC 237 (21e), BC 382 (21e), BC 582 (21e)	kompl.: BC 557
BC 548 (V, A, B, C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni, 30V, 0,2A, 0,5W 300MHz, B=75-900	BC 108 (4a), BC 172 (21e), BC 183 (21e), BC 208 (4), BC 238 (21e), BC 383 (21e), BC 583 (21e)	kompl.: BC 558
BC 549 (B, C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni-re, 30V, 0,2A, 0,5W 300 MHz, B=240-800	BC 109 (4a), BC 171 (21e), BC 184 (21e), BC 209 (4), BC 239 (21e), BC 384 (21e), BC 584 (21e)	kompl.: BC 559
BC 550 (B, C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-NPN	21e	Uni-re, 50V, 0,2A, 0,5W 300 MHz, B=240-900	BC 184 (21e), BC 384 (21e), BC 414 (21e)	kompl.: BC 560
BC 556 (V, A, B)	AEG, ITT, MUL, PHI, SIE, VAL	Si-PNP	21e	Uni, 80V, 0,2A, 0,5W 150 MHz, B=125-500	BC 256 (21e), BC 266 (4a), BC 448 (21e)	kompl.: BC 546
BC 557 (V, A, B)	AEG, ITT, MUL, PHI, SIE, VAL	Si-PNP	21e	Uni, 50V, 0,2A, 0,5W 150 MHz, B=125-500	BC 177 (4a), BC 204 (4), BC 212 (21e), BC 512 (21e)	BC 251 (21e), BC 307 (21e), kompl.: BC 547
BC 558 (V, A, B, C)	AEG, ITT, MUL, PHI, SIE, VAL	Si-PNP	21e	Uni 30V, 0,2A, 0,5W 150MHz, B=75-900	BC 178 (4a), BC 205 (4), BC 213 (21e), BC 513 (21e)	BC 252 (21e), BC 308 (21e), kompl.: BC 548

JFETS

table 15
case: **TO18**



PIN VIEW

(B) 1. Source 2. Drain 3. Gate
(C) 1. Source 2. Gate 3. Drain
(D) 1. Drain 2. Source 3. Gate

Maximum ratings at 25°C ambient temperature (unless otherwise stated)

type	channel	P_D (max.)	V_{GS} (off) (max.)	V_{DS} (max.)	V_{DG} (max.)	I_{DSS} (min.)	I_{DSS} (max.)	C_{iss} (typ.)	t_r (typ.)	t_f (typ.)	connection	application
2N4092	N	1·8 W (T_A = 25 °C)	7 V	40 V	40 V	15 mA	—	16 pF (max.)	20 ns	—	B	Switching
2N4391	N	1·8 W	-10 V	40 V	—	50 mA	100 pA	14 pF	5 ns	15 ns	B	Switching
2N4392	N	1·8 W	-5 V	40 V	—	25 mA	100 pA	14 pF	5 ns	20 ns	B	Switching
2N4393	N	1·8 W (T_C = 25 °C)	-3 V	40 V	40 V	5 mA	100 pA	14 pF (max.)	5 ns	30 ns	B	Switching
2N4858	N	1·8 W	-4 V	-40 V	—	8 mA	250 pA	18 pF (max.)	10 ns (max.)	—	D	Switching
2N4858A	N	360 mW (T_A = 25 °C)	-4 V	40 V	40 V	8 mA	250 pA	10 pF (max.)	8 ns	—	D	Switching
2N4859A	N	360 mW (T_A = 25 °C)	-10 V	30 V	30 V	50 mA	250 pA	10 pF (max.)	3 ns	—	D	Switching
2N4860A	N	360 mW (T_A = 25 °C)	-6 V	30 V	30 V	20 mA	250 pA	10 pF (max.)	4 ns	—	D	Switching
2N4861	N	360 mW (T_A = 25 °C)	-4 V	30 V	30 V	8 mA	250 pA	18 pF (max.)	10 ns	—	C	Switching

table 16
case: **TO72**

PIN VIEW

(C) 1. Source 2. Drain 3. Gate 4. Case
(D) 1. Source 2. Gate 3. Drain 4. Case

Maximum ratings at 25°C Ambient temperature (unless otherwise stated)

type	channel	P_D (max.)	V_{GS}(th) (max.)	V_{DG} (max.)	V_{DS} (max.)	I_{DSS} (min.)	I_{DSS} (max.)	Y_{fs} (min.)	C_{iss} (typ.)	t_r (typ.)	t_f (typ.)	I_D (max.)	connection	application
2N4118	N	300 mW	-3 V	-40 V	—	8 pA	10 pA	—	3 pF (max.)	—	—	—	D	General purpose amp
2N4220	N	300 mW (T_A = 25 °C)	-4 V	30 V	30 V	0·5 mA	100 pA	1 mS	4·5 pF	—	—	15 mA	C	Low noise
2N4351	N	300 mW (T_A = 25 °C)	-5 V	30 V	25 V	10 nA (max.)	10 pA	1 mS	5 pF (max.)	65 ns	100 ns	30 mA	D	Switching
2N4416	N	300 mW (T_A = 25 °C)	-6 V	35 V	30 V	5 mA	100 pA	4 mS	4 pF (max.)	—	—	—	C	VHF/UHF amplifier

table 17
case: **TO92**

PIN VIEW

(D) 1. Drain 2. Gate 3. Source
(E) 1. Gate 2. Source 3. Drain
(F) 1. Gate 2. Drain 3. Source
(G) 1. Source 2. Gate 3. Drain

Maximum ratings at 25°C Ambient temperature (unless otherwise stated)

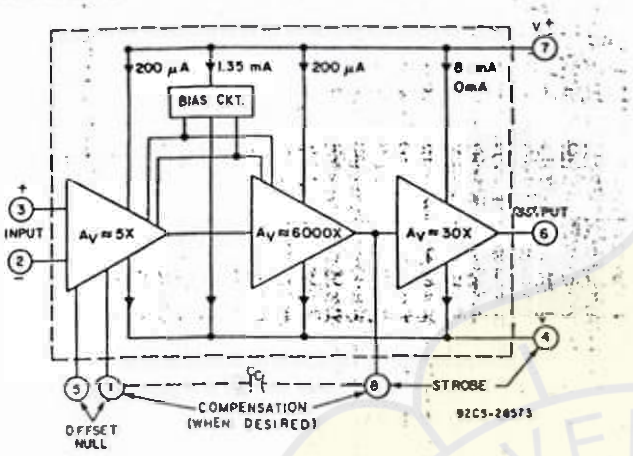
type	channel	P_D (max.)	V_{GS}(th) (max.)	V_{DG} (max.)	V_{DS} (max.)	I_{DSS} (min.)	I_{DSS} (max.)	Y_{fs} (min.)	C_{iss} (typ.)	t_r (typ.)	t_f (typ.)	I_D (max.)	connection	application
BF 244A	N	360 mW (T_A = 25 °C)	—	30 V	30 V	2 mA	5 nA	3 mS	3 pF	—	—	100 mA	D	VHF/UHF amplifier
BF 245A	N	360 mW (T_A = 25 °C)	—	30 V	30 V	2 mA	5 nA	3 mS	3 pF	—	—	100 mA	D	VHF/UHF amplifier
BS107	N	600 mW (T_C = 25 °C)	—	—	200 V	30 nA (max.)	10 nA	—	72 pF	—	—	250 mA	G	Switching
BS170	N	830 mW (T_C = 25 °C)	—	—	60 V	—	10 nA	—	60 pF	-	-	500 mA	G	Switching
2N3819	N	200 mW (T_A = 25 °C)	-8 V	25 V	25 V	2 mA	2 nA	2 mS	8 pF (max.)	—	—	—	D	General purpose amplifier
2N5457	N	310 mW	-6 V	25 V	25 V	1 mA	1 nA	1 mS	7 pF (max.)	—	—	10 mA	E	General purpose amplifier
2N5486	N	310 mW (T_C = 25 °C)	-6 V	25 V	—	8 mA	1 nA	4 mS	5 pF (max.)	—	—	—	E	VHF/UHF amplifier
J112	N	360 mW	—	-35 V	—	5 mA	1 nA	—	—	6 ns	15 ns	—	E	Switching
J309	N	360 mW	-4 V	-25 V	-25 V	12 mA	1 nA	10 mS	—	—	—	—	E	VHF/UHF amplifier
J310	N	360 mW	-6·5 V	-25 V	-25 V	24 mA	1 nA	8 mS	—	—	—	—	E	VHF/UHF amplifier
2N3820	P	200 mW (T∅ = 25 °C)	8 V	-20 V	-20 V	-0·3 mA	20 nA	0·8 mS	32 pF (max.)	—	—	—	D	General purpose amplifier
2N5460	P	3hW	6 V	-40 V	—	-1 mA	5 nA	1 mS	7 pF (max.)	—	—	—	F	Low noise amplifier
2N5461	P	310 mW	7·5 V	-40 V	—	-2 mA	500 nA	1·5 mS	7 pF (max.)	—	—	—	E	Low noise amplifier
J175	P	350 mW	6 V	30 V	—	-7 mA	1 nA	—	—	10 ns	25 ns	-	G	Switching
J177	P	350 mW	2·25 V	30 V	—	15 mA	1 nA	—	—	25 ns	25 ns	-	G	Switching

Re fer to pages 686 et seq for pricing information

For a full selection of Component Manufacturer's Data Books refer to the Technical Library section

BiMOS Operational Amplifiers

CA3130, CA3130A, CA3130B MOS/FET Input, CMOS Output
CA3160, CA3160A, CA3160B Frequency Compensated Version of CA3130
CA3260, CA3260A, CA3260B Dual Version of CA3160



Type No.	Package	Operating Temp. Range
CA3130S, AS, BS CA3160S, AS, BS CA3260S, AS, BS	8-Lead DIL-CAN	
CA3130T, AT, BT CA3160T, AT, BT CA3260T, AT, BT	8-Lead TO-5	
CA3130E, AE CA3160E, AE CA3260E, AE	8-Lead Mini-DIP	−55 to + 125° C
CA3130H CA3160H CA3260H	Chip	

Gate-protected p-channel MOS/FET (PMOS) transistors in the input circuit provide very-high-input impedance, very-low-input current, exceptional speed performance, and common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

Features:

- MOS/FET input stage provides:
  very high $Z_i = 1.5\ T\Omega$ ($1.5 \times 10^{12}\Omega$) typ.
  very low $I_i = 5$ pA typ. at 15-V operation
  $= 2$ pA typ. at 5-V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails
- Wide BW: 15 MHz typ. (unity-gain bandwidth) - CA3130
  4 MHz typ. (unity-gain bandwidth) - CA3160, CA3260
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor - CA3130
- Internal phase compensation for unity gain (With terminal access for supplementary external phase compensation network if desired) - CA3160
- Low V_{IO}: 2 mV max. (CA3160, CA3260)

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators
- High-input-impedance wideband amplifiers
- Voltage followers
- Voltage regulators
- Peak detectors - CA3130
- Single-supply full-wave precision rectifiers - CA3130
- Photo-diode sensor amplifiers
- Wien-Bridge oscillators
- Voltage-controlled oscillators
- Ideal interface with digital COS/MOS

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

Electrical Characteristics: $T_A = 25°C, V^+ = 7.5\ V, V^- = -7.5\ V$

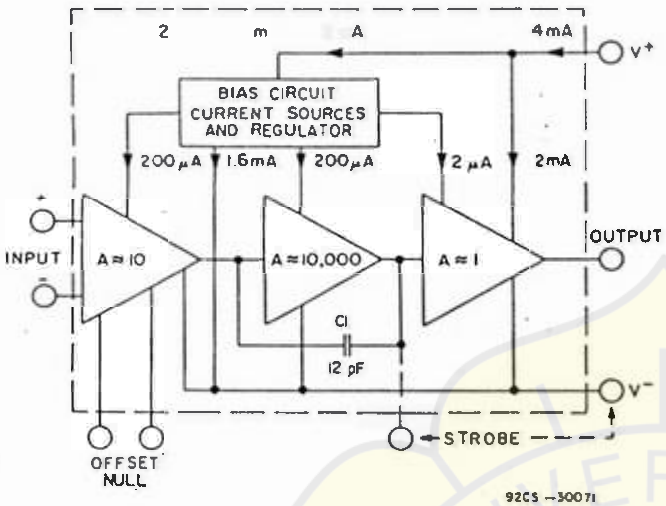
Type	R_i (Typ) TΩ	I_i (Max) pA	I_O (Max) pA	V_{IO} (Max) mV	SR (Typ) V/μs	f_t (Typ) MHz	Output Swing (Typ)-V	Compensation	A_{OL} (min.) V/V	A_{OL} (min.) dB	Supply Voltage Range V
CA3130	1.5	50	30	15	10	4	−0.002 to + 13	External	50K	94	4.5 to 16
CA3130A	1.5	30	20	5	10	4	−0.002 to + 13	External	50K	94	4.5 to 16
CA3130B	1.5	20	10	2	10	4	−0.002 to + 13	External	100K	100	4.5 to 16
CA3160	1.5	50	30	15	10	4	−0.002 to + 13	Internal	50K	94	4.5 to 16
CA3160A	1.5	30	20	5	10	4	−0.002 to + 13	Internal	50K	94	4.5 to 16
CA3160B	1.5	20	10	2	10	4	−0.002 to + 13	Internal	100K	100	4.5 to 16
CA3260*	1.5	50	30	15	10	4	−0.002 to + 13	Internal	50K	94	4 to 16
CA3260A*	1.5	30	20	5	10	4	−0.002 to + 13	Internal	50K	94	4 to 16
CA3260B*	1.5	20	10	2	10	4	−0.002 to + 13	Internal	100K	100	4 to 16

*Characteristics are for each amplifier.

BiMOS Operational Amplifiers

CA3140, CA3140A, CA3140B
CA3240, CA3240A

MOS/FET Input, Bipolar Output
Dual Version of CA3140



Type No.	Package	Operating Temp. Range
CA3140S, AS, BS	8-Lead DIL-CAN	−55 to + 125° C
CA3140T, AT, BT	8-Lead TO-5	−55 to + 125° C
CA3140E, AE	8-Lead Mini-DIP	−55 to + 125° C
CA3240E, AE		−40 to + 85° C
CA3240E1, AE1	14-Lead DIP	−40 to + 85°C
CA3140H	Chip	−55 to + 125° C
CA3240H		−40 to + 85° C

The CA3140 and CA3240 Series of BiMOS op amps give you the big advantage of MOS/FET input... plus bipolar speed and high supply voltage operating capability: 4 to 44V, dual or single supply. Wide common-mode input voltage range - can be swung 0.5 V below negative rail. Output swing complements input common-mode range, permitting full utilization of low supply voltages (down to 4V). And PMOS input devices are protected by rugged bipolar diodes.

Features:

- MOS/FET Input Stage
  - (a) Very high input impedance (Z_{IN}) - 1.5 T Ωtyp.
  - (b) Very low input current (I_I) - 10 pA typ. at ± 15V
  - (c) Low input-offset voltage (V_{IO}) - to 2 mV max.
  - (d) Wide common-mode input-voltage range (V_{ICR}) - can be swung 0.5 volt below negative supply-voltage rail
  - (e) Output swing complements input common-mode range
- Rugged input stage - bipolar diode protected
- Directly replaces industry type 741 (CA3140) or 747 (CA3240) in most applications
- Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)
- Operation from 4-to-44 volts
- Single or Dual supplies
- Internally compensated
- Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts
- Wide bandwidth - 4.5 MHz unity gain at ± 15V or 30V; 3.7 MHz at 5V
- High voltage-follower slew rate - 9 V/μs
- Fast settling time - 1.4μs typ. to 10 mV with a 10-V_{p-p} signal
- Output swings to within 0.2 volt of negative supply
- Strobable output stage

Applications

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample-and-hold amplifiers
- Long-duration timers/multivibrators (microseconds-minutes-hours)
- Photocurrent instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5-V TTL systems & other low-supply voltage systems
- All standard operational amplifier applications
- Function generators
- Tone controls
- Power supplies
- Portable instruments
- Intrusion alarm systems

Electrical Characteristics: $T_A = 25°C, V^+ = 15V, V^- = -15V$

Type	R_I (Typ) TΩ	I_I (Max) pA	I_{IO} (Max) pA	V_{IO} (Max) mV	SR (Typ) V/μs	f_T (Typ) MHz	Output Swing (Typ)-V	Compensation	A_{OL} (min.) V/V	A_{OL} (min.) dB	Supply Voltage Range V
CA3140	1.5	50	30	15	9	4.5	−14 to + 13	Internal	20K	86	4 to 36
CA3140A	1.5	40	20	5	9	4.5	−14 to + 13	Internal	20K	86	4 to 36
CA3140B	1.5	30	10	2	9	4.5	−14 to +13	Internal	50K	94	4 to 44
CA3240	1.5	50	30	15	9	4.5	−14 to + 13	Internal	20	86	4 to 36
CA3240A	1.5	40	20	5	9	4.5	−14 to +13	Internal	20	86	4 to 36

CMOS Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 2).

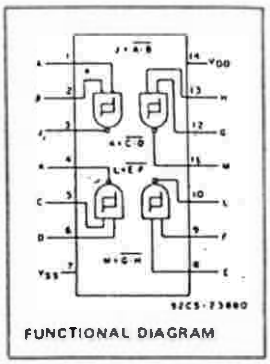
The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at V_{DD} = 5 V and 2.3 V at V_{DD} = 10 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (T_A=Full Package-Temp. Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)		−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS		−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT		±10 mA
POWER DISSIPATION PER PACKAGE (P_D):		
For T_A = −40 to +60°C (PACKAGE TYPE E)		500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW	
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)		500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D,F,K)	Derate Linearly at 12 mW/°C to 200 mW	
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)		100 mW
OPERATING-TEMPERATURE RANGE (T_A):		
PACKAGE TYPES D, F, K, H		−55 to +125°C
PACKAGE TYPE E		−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})		−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.		+265°C

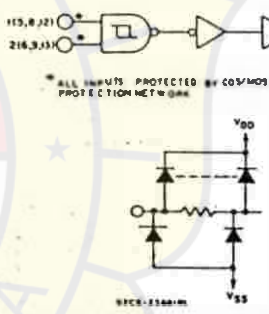


Fig. 1 – Logic diagram – 1 of 4 Schmitt triggers.

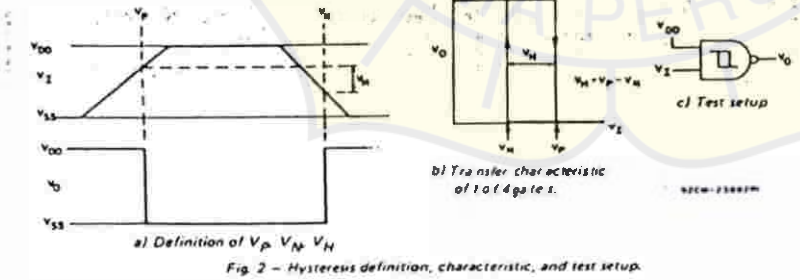


Fig. 2 – Hysteresis definition, characteristic, and test setup.

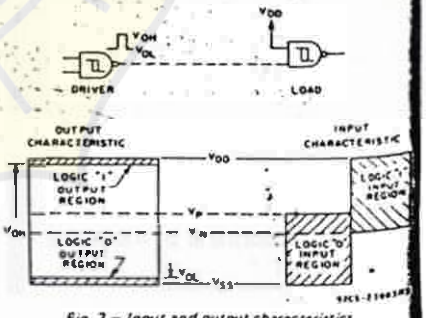


Fig. 3 – Input and output characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,F,K,H Packages Values at -40, +25, +85 Apply to E Packages							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	MIN.	TYP.	MAX.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	1	1	30	30	-	0.02	1	μA
	-	0,10	10	2	2	60	60	-	0.02	2	
	-	0,15	15	4	4	120	120	-	0.02	4	
	-	0,20	20	20	20	600	600	-	0.04	20	
Positive Trigger Threshold Voltage V_P Min.	-	a	5	2.2	2.2	2.2	2.2	2.2	2.9	-	V
	-	a	10	4.6	4.6	4.6	4.6	4.6	5.9	-	
	-	a	15	6.8	6.8	6.8	6.8	6.8	8.8	-	
	-	b	5	2.6	2.6	2.6	2.6	2.6	3.3	-	
	-	b	10	5.6	5.6	5.6	5.6	5.6	7	-	
	-	b	15	6.3	6.3	6.3	6.3	6.3	9.4	-	
V_P Max.	-	a	5	3.6	3.6	3.6	3.6	-	2.9	3.6	V
	-	a	10	7.1	7.1	7.1	7.1	-	5.9	7.1	
	-	a	15	10.8	10.8	10.8	10.8	-	8.8	10.8	
	-	b	5	4	4	4	4	-	3.3	4	
	-	b	10	8.2	8.2	8.2	8.2	-	7	8.2	
	-	b	15	12.7	12.7	12.7	12.7	-	9.4	12.7	
Negative Trigger Threshold Voltage V_N Min.	-	a	5	0.9	0.9	0.9	0.9	0.9	1.9	-	V
	-	a	10	2.5	2.5	2.5	2.5	2.5	3.9	-	
	-	a	15	4	4	4	4	4	5.8	-	
	-	b	5	1.4	1.4	1.4	1.4	1.4	2.3	-	
	-	b	10	3.4	3.4	3.4	3.4	3.4	5.1	-	
	-	b	15	4.8	4.8	4.8	4.8	4.8	7.3	-	
V_N Max.	-	a	5	2.8	2.8	2.8	2.8	-	1.9	2.8	V
	-	a	10	5.2	5.2	5.2	5.2	-	3.9	5.2	
	-	a	15	7.4	7.4	7.4	7.4	-	5.8	7.4	
	-	b	5	3.2	3.2	3.2	3.2	-	2.3	3.2	
	-	b	10	6.6	6.6	6.6	6.6	-	5.1	6.6	
	-	b	15	9.6	9.6	9.6	9.6	-	7.3	9.6	
Hysteresis Voltage V_H Min.	-	a	5	0.3	0.3	0.3	0.3	0.3	0.9	-	V
	-	a	10	1.2	1.2	1.2	1.2	1.2	2.3	-	
	-	a	15	1.6	1.6	1.6	1.6	1.6	3.5	-	
	-	b	5	0.3	0.3	0.3	0.3	0.3	0.9	-	
	-	b	10	1.2	1.2	1.2	1.2	1.2	2.3	-	
	-	b	15	1.6	1.6	1.6	1.6	1.6	3.5	-	
V_H Max.	-	a	5	1.6	1.6	1.6	1.6	-	0.9	1.6	V
	-	a	10	3.4	3.4	3.4	3.4	-	2.3	3.4	
	-	a	15	5	5	5	5	-	3.5	5	
	-	b	5	1.6	1.6	1.6	1.6	-	0.9	1.6	
	-	b	10	3.4	3.4	3.4	3.4	-	2.3	3.4	
	-	b	15	5	5	5	5	-	3.5	5	

[a] Input on terminals 1,5,8,12 or 2,6,9,13, other inputs at $0V_{DD}$

[b] Inputon terminals 1 and 2 or 6, 8 and 9, or 12 and 13, other inputs at $0V_{DD}$

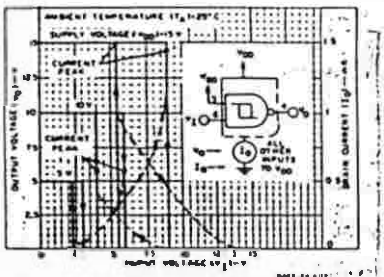


Fig. 4 – Typical current and voltage transfer characteristics.

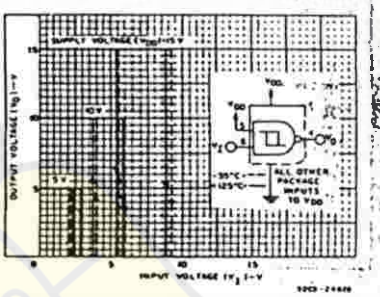


Fig. 5 – Typical voltage transfer characteristics as a function of temperature.

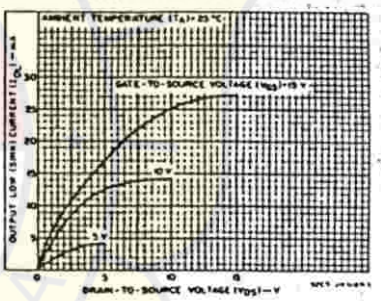


Fig. 6 – Typical output low (sink) current characteristics.

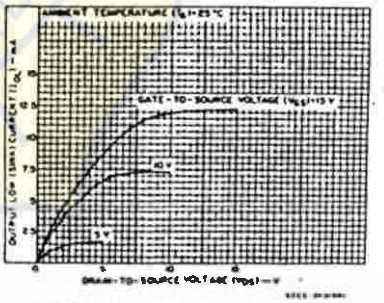


Fig. 7 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS (CONT'D)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Output Low (Sink) Current, I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage Low Level, V_{OL} Max.	–	0.5	5	0.05				–	0	0.05	V
	–	0.10	10	0.05				–	0	0.05	
	–	0.15	15	0.05				–	0	0.05	
Output Voltage High Level, V_{OH} Min.	–	0.5	5	4.95				4.95	5	–	
	–	0.10	10	9.95				9.95	10	–	
	–	0.15	15	14.95				14.95		–	
Input Current, I_{IN} Max.	–	0.18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

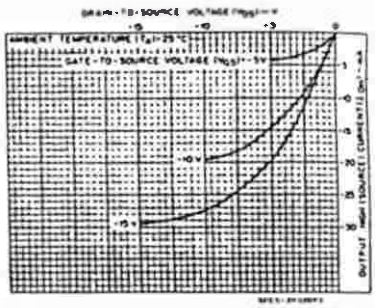


Fig. 8 – Typical output high (source) current characteristics.

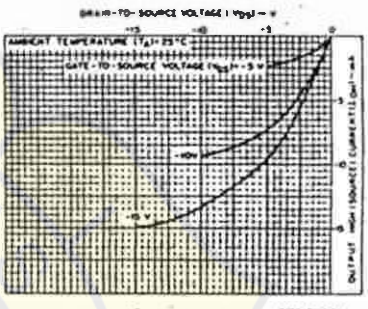


Fig. 9 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH}	5	190	380	ns
	10	90	180	
	15	65	130	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

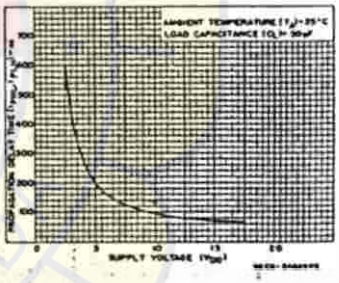


Fig. 10 – Typical propagation delay time vs. supply voltage.

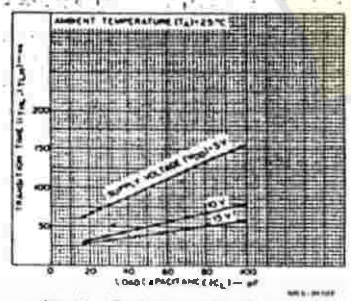


Fig. 11 – Typical transition time vs. load capacitance.

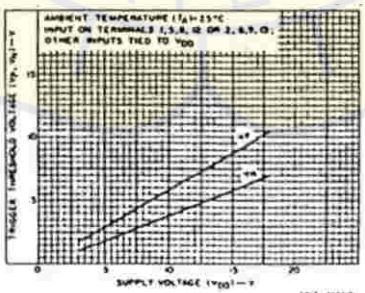


Fig. 12 – Typical trigger threshold voltage vs. V_{DD}

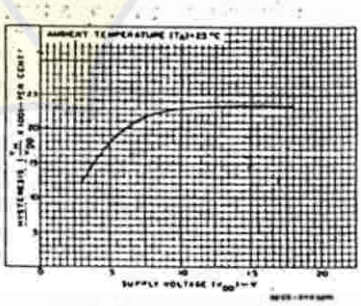
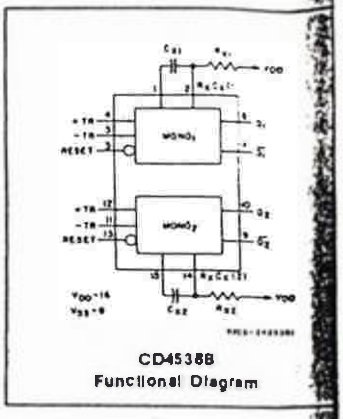


Fig. 13 Typical per cent hysteresis vs. supply voltage.

CMOS Dual Precision Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

Features:
- *Retriggerable/resettable capability*
- *Trigger and reset propagation delays independent of R_x, C_x*
- *Triggering from leading or trailing edge*
- *Q and $\overline{Q}$ buffered outputs available*
- *Separate resets*
- *Wide range of output-pulse widths*
- *Schmitt trigger input allows unlimited rise and fall times on +TR and −TR inputs*



CD4538B
Functional Diagram

The RCA-CD4538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_x) and an external capacitor (C_x) control the timing and accuracy for the circuit. Adjustment of R_x and C_x provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_x and C_x. Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4538B is not used, its inputs must be tied to either V_{DD} or V_{SS}. See Table I.

In normal operation the circuit retriggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used. The time period (T) for this multivibrator can be calculated by: $T = R_x C_x$.

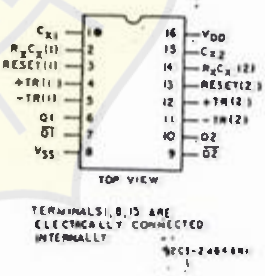
The minimum value of external resistance, R_x, is 4 KΩ. The maximum and minimum values of external capacitance, C_x, are 100 μF and 5000 pF, respectively.

The CD4538B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD4538B is similar to type MC14538 and is pin-for-pin compatible with the CD4098B.

- *100% tested for maximum quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C*
- *Noise margin (full package-temperature range):*
  1 V at V_{DD}=5 V
  2 V at V_{DD}=10 V
  2.5 V at V_{DD}=15 V
- *5-V, 10-V, and 15-V parametric ratings*
- *Standardized, symmetrical output characteristics*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."*

Applications:
- *Pulse delay and timing*
- *Pulse shaping*



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D,F,K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D,F,K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E ..... -40 to +85°C
PACKAGE TYPE D,F,K,H ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

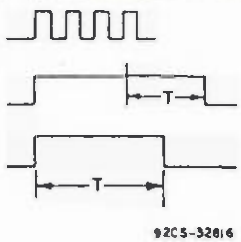
RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS		UNITS
			Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		—	3	18	V
Input Pulse Width +TR, -TR, or RESET	t_{WH}, t_{WL}	5	140	—	ns
		10	80	—	
		15	60	—	

TABLE I
CD4538B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V_{DD} TO TERM. NO.		V_{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:
1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.



92CS-32816

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,F,K, H Pkgs. Values at -40, +25, +85 Apply to E Pkgs.							UNIT
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	+25 Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

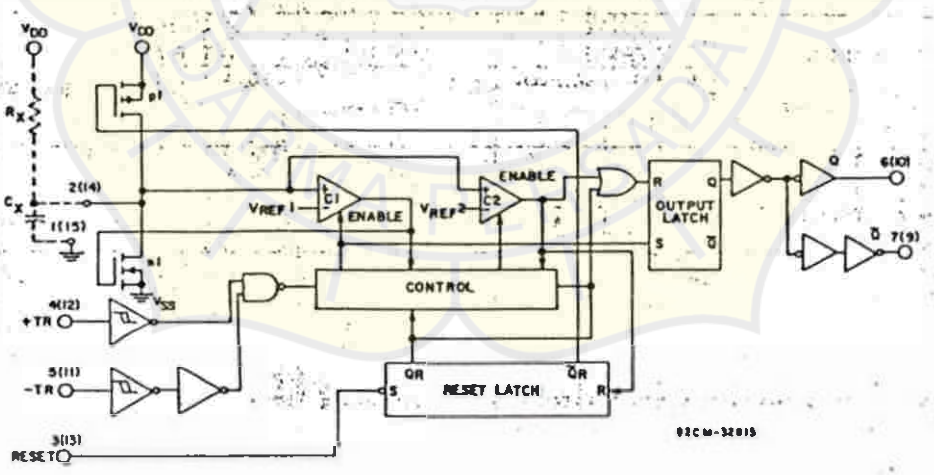


Fig. 1 - Logic diagram (⅓ of device shown).

DYNAMIC ELECTRICAL CHARACTERISTICS, At T_A=25° C; Input t_r,t_f=20 ns, C_L=50 pF

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Transition Time	t_{TLH}, t_{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time: +TR or -TR to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	5	—	300	600	
		10	—	150	300	
		15	—	100	220	
Reset to Q or $\overline{Q}$		5	—	250	500	
		10	—	125	250	
		15	—	95	190	
Minimum Input Pulse Width: +TR,-TR or Reset	t_{WH}, t_{WL}	5	—	80	140	
		10	—	40	80	
		15	—	30	60	
Output Pulse Width - Q or $\overline{Q}$: C_x=0.005 μF, R_x=10KΩ*	T	5	57	60.6	64.5	μs
		10	55	58.9	63.0	
		15	55	59.1	63.5	
C_x=0.1μF, R_x=100KΩ		5	9.4	9.97	10.5	ms
		10	9.4	9.95	10.6	
		15	9.5	10.00	10.6	
C_x=10 μF, R_x=100 KΩ		5	0.95	1.00	1.06	s
		10	0.95	1.00	1.06	
		15	0.96	1.01	1.07	
Pulse Width Match between circuits in same package: C_x=0.1μF, R_x=100 KΩ	$\frac{100\ (T_1-T_2)}{T_1}$	5	—	±1	—	%
		10	—	±1	—	
		15	—	±1	—	
Minimum Retrigger Time	t_{rr}	5	0	—	—	ns
		10	0	—	—	
		15	0	—	—	
Input Capacitance	C_{IN}	Any Input	—	5.0	7.5	pF

*Note: Minimum R_x value=4 KΩ, minimum C_x value=5000 pF.

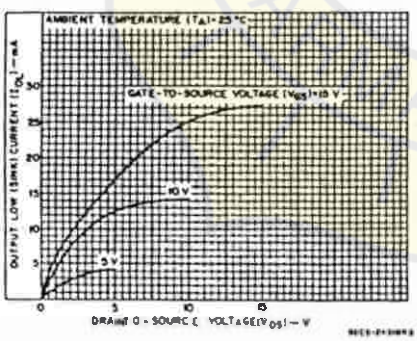


Fig. 2 - Typical output low (sink) current characteristics.

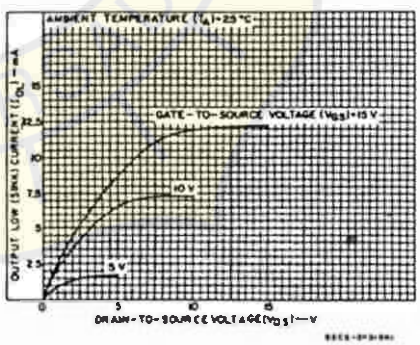


Fig. 3 - Minimum output low (sink) current characteristics.

CD4017B, CD4022B Types

CMOS Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4017B—Decade Counter with 10 Decoded Outputs

CD4022B—Octal Counter with 8 Decoded Outputs

The RCA CD4017B and CD4022B are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017B or every 8 clock input cycles in the CD4022B and is used to ripple-clock the succeeding device in a multi-device counting chain.

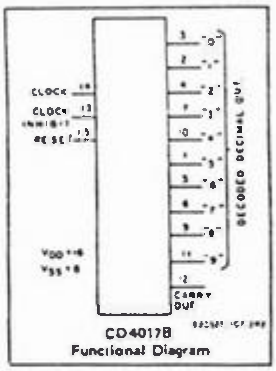
The CD4017B and CD4022B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages(K suffix), and in chip form (H suffix).

Features:

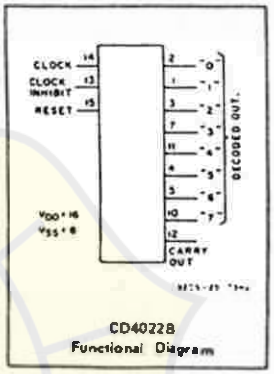
- Fully static operation
- Medium-speed operation . . . 10 MHz (typ.) at V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Decade counter/decimal decode display (CD4017B)
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide-by-N counting
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"



CD4017B
Functional Diagram



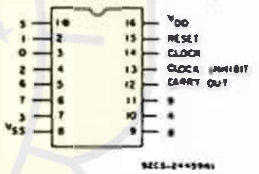
CD4022B
Functional Diagram

RECOMMENDED OPERATING CONDITIONS

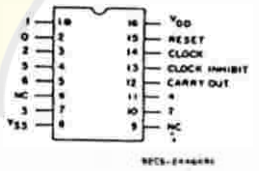
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Clock Input Frequency, f_{CL}	5	–	2.5	MHz
	10	–	5	
	15	–	5.5	
Clock Pulse Width, t_W	5	200	–	ns
	10	90	–	
	16	60	–	
Clock Rise & Fall Time, t_{rCL}, t_{fCL}	5	UNLIMITED*		
	10			
	15			
Clock Inhibit Setup Time, t_s	5	230	–	ns
	10	100	–	
	15	70	–	
Reset Pulse Width, t_{WR}	5	260	–	ns
	10	110	–	
	15	60	–	
Reset Removal Time, t_{rem}	5	400	–	ns
	10	280	–	
	15	150	–	

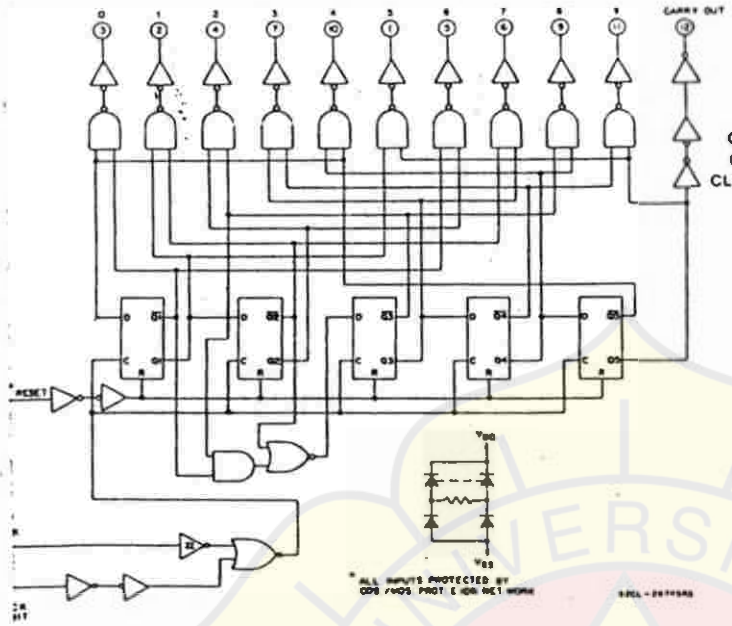
*Operation is also possible with zero clock rise and fall time. If Pin 13 is used as the clock input and Pin 14 is tied high (for advancing count on negative transition of the clock), rise and fall time should be ≤ 15 μs.



TOP VIEW
CD4017B
TERMINAL DIAGRAM



TOP VIEW
NC = no connection
CD4022B
TERMINAL DIAGRAM



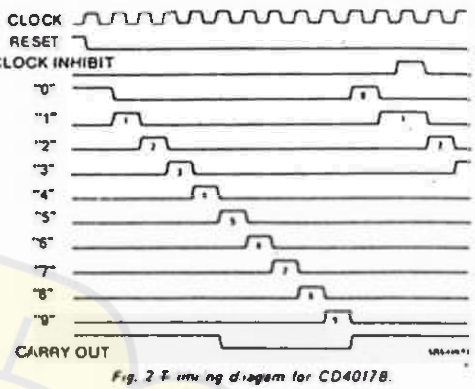


Fig. 2 Timing diagram for CD4017B.

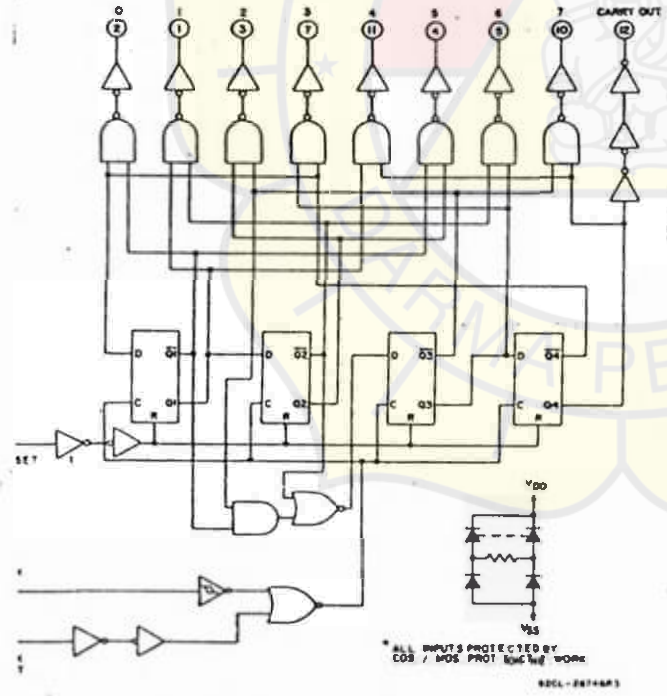


Fig. 3 – Logic diagram for CD4022B.

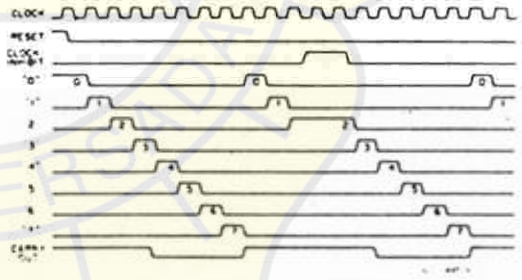


Fig. 4 – Timing diagram for CD4022B.

CD4017B, CD4022B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

VOLTAGE REFERENCED TO V_{SS} TERMINAL(S) ..... -0.5 to +20 V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... -55 to +125°C

PACKAGE TYPE E ..... -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C

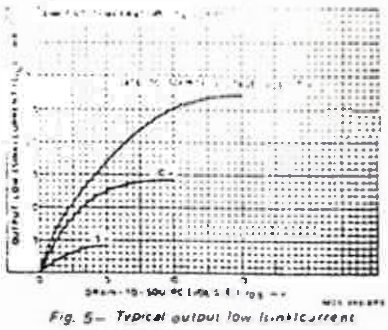


Fig. 5— Typical output low (sink) current characteristics.

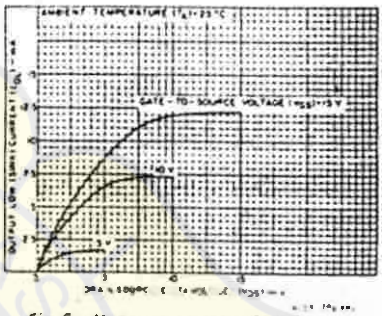


Fig. 6— Minimum output low (sink) current characteristics.

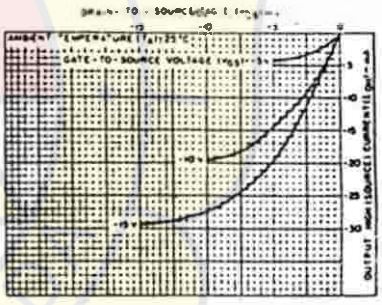


Fig. 7— Typical output high (source) current characteristics.

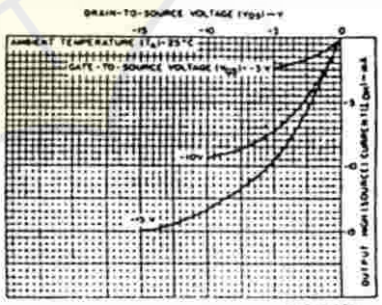


Fig. 8— Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H, Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	5	5	150	150	-	0.04	5	µA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage Low Level, V_{OL} Max	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage High Level, V_{OH} Min.	-	0,5	5	4.95				4.95	5	-	
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage V_{IL} Max	10.5, 4.5	-	5	1.5				-	-	1.5	
	1,9	-	10	3				-	-	3	
	15, 13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	-	5	3.5				3.5	-	-	
	1,9	-	10	7				7	-	-	
	15, 13.5	-	15	11				11	-	-	
Input Current I_{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	µA

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25 °C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CLOCKED OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Decode Out	5	–	325	650	ns
	10	–	135	270	
	15	–	85	170	
Carry Out	5	–	300	600	
	10	–	125	250	
	15	–	80	160	
Transition Time, t_{THL}, t_{TLH} Carry Out or Decode Out Line	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency, f_{CL}*	5	2.5	5	–	MHz
	10	5	10	–	
	15	5.5	11	–	
Minimum Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	45	90	
	15	–	30	60	
Clock Rise or Fall Time, t_rCL, t_fCL	5, 10, 15	UNLIMITED			
Minimum Clock Inhibit to Clock Setup Time, t_s	5	–	115	230	ns
	10	–	50	100	
	15	–	35	70	
Input Capacitance, C_{IN}	Any Input	–	5	–	pF
RESET OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Carry Out or Decode Out Lines	5	–	265	530	ns
	10	–	115	230	
	15	–	85	170	
Minimum Reset Pulse Width, t_W	5	–	130	260	ns
	10	–	55	110	
	15	–	30	60	
Minimum Reset Removal Time	5	–	200	400	ns
	10	–	140	280	
	15	–	75	150	

* Measured with respect to carry output line.

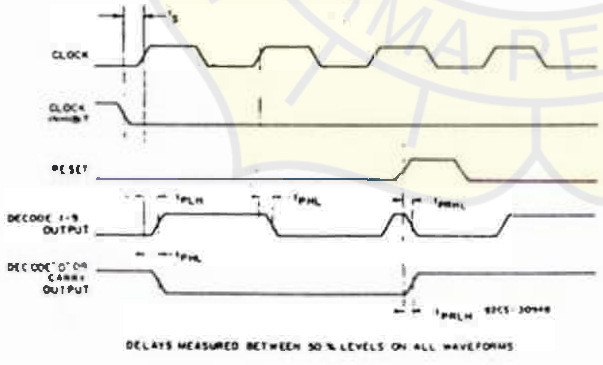


Fig. 9 – Propagation delay, setup, and hold time waveforms.

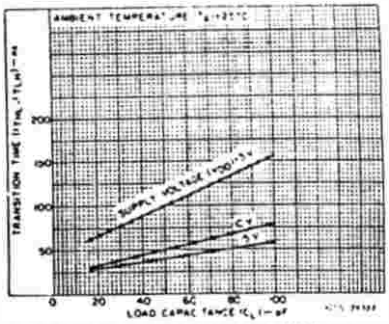


Fig. 10 – Typical transition time as a function of load capacitance.

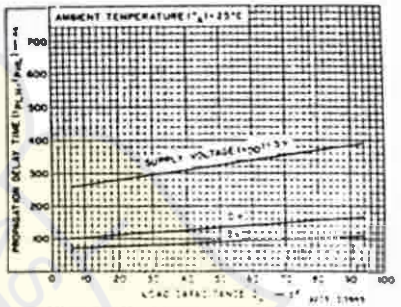


Fig. 11 – Typical propagation delay time as a function of load capacitance (clock to decode output).

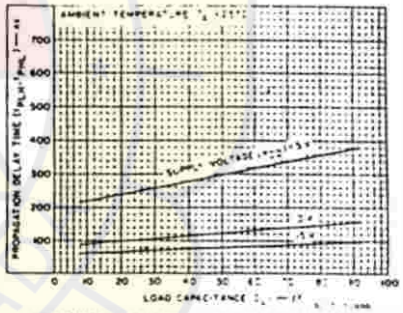


Fig. 12 – Typical propagation delay time as a function of load capacitance (clock to carry out).

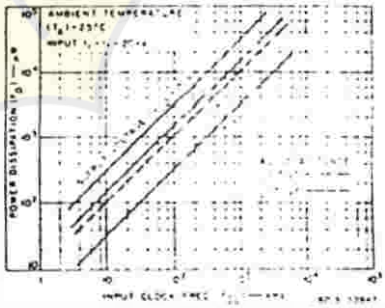


Fig. 13 – Typical dynamic power dissipation as a function of clock input frequency.

μA7800 SERIES
3-TERMINAL POSITIVE VOLTAGE REGULATORS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

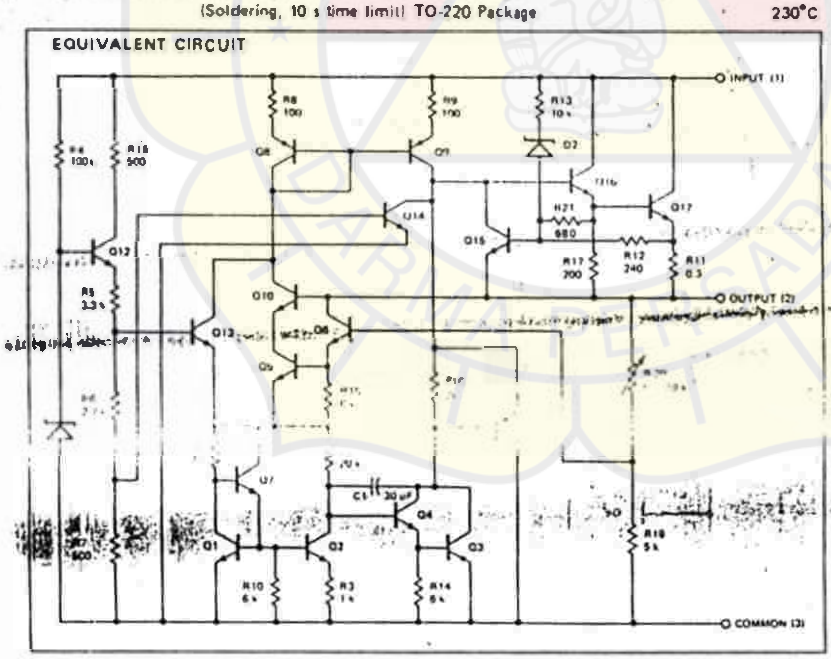
GENERAL DESCRIPTION — The μA7800 series of monolithic 3-Terminal Positive Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current-limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1 A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- OUTPUT CURRENT IN EXCESS OF 1 A
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE AREA COMPENSATION
- AVAILABLE IN THE TO-220 AND THE TO-3PACKAGE
- OUTPUT VOLTAGES OF 5, 6, 8, 8.5, 12, 15, 18, AND 24 V

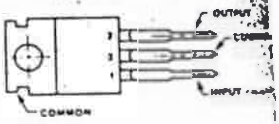
ABSOLUTE MAXIMUM RATINGS

Input Voltage (5 V through 18 V)		35 V
(24V)		40 V
Internal Power Dissipation		Internally Limited
Storage Temperature Range		−65°C to +150°C
Operating Junction Temperature Range	μA7800	−55°C to +150°C
	μA7800C	0°C to +150°C
Lead Temperature (Soldering, 60 s time limit) TO-3 Package		300°C
(Soldering, 10 s time limit) TO-220 Package		230°C

EQUIVALENT CIRCUIT



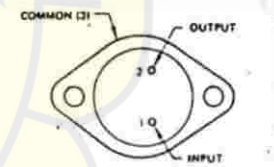
CONNECTION DIAGRAMS
TO-220 PACKAGE
(SIDE VIEW)



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA7805C	μA7805UC
6 V	μA7806C	μA7806UC
8 V	μA7808C	μA7808UC
8.5 V	μA7885C	μA7885UC
12 V	μA7812C	μA7812UC
15V	μA7815C	μA7815UC
18 V	μA7818C	μA7818UC
24V	μA7824C	μA7824UC

TO-3PACKAGE
(TOP VIEW)



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA7805	μA7805KM
6 V	μA7806	μA7806KM
8 V	μA7808	μA7808KM
8.5 V	μA7885	μA7885KM
12 V	μA7812	μA7812KM
15 V	μA7815	μA7815KM
18 V	μA7818	μA7818KM
24V	μA7824	μA7824KM
5 V	μA7805C	μA7805KC
6V	μA7806C	μA7806KC
8 V	μA7808C	μA7808KC
8.5V	μA7885C	μA7885KC
12 V	μA7812C	μA7812KC
15V	μA7815C	μA7815KC
18 V	μA7818C	μA7818KC
24 V	μA7824C	μA7824KC

*Planar is a patented Fairchild process.

μA 780 8

ELECTRICAL CHARACTERISTICS: V_{IN} = 14 V, I_{OUT} = 500 mA, −55° C ≤ T_J ≤ 150 °C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF,

MAX.	CHARACTERISTICS		CONDITIONS		MIN.	TYP.	MAX.	UNITS
6.25	Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
60	Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	80	mV
30				11 V ≤ V_{IN} ≤ 17 V		2.0	40	mV
100	Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	100	mV
30				250 mA ≤ I_{OUT} ≤ 750 mA		4.0	40	mV
8.35	Output Voltage		11.5 V ≤ V_{IN} ≤ 23 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		7.6		8.4	V
6.0	Quiescent Current		T_J = 25°C			4.3	6.0	mA
0.8	Quiescent Current Change	with line	11.5 V ≤ V_{IN} ≤ 25 V				0.8	mA
0.5		with load	5 mA ≤ I_{OUT} ≤ 1.0A				0.5	mA
40	μV	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
5		Ripple Rejection	f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		62	72		dB
2		Dropout Voltage	I_{OUT} = 1.0 A, T_J = 25°C			2.0	2.5	V
3		Output Resistance	f = 1 kHz			16		mΩ
1		Short Circuit Current	T_J = 25°C, V_{IN} = 35 V			0.75	1.2	A
	mV/	Peak Output Current	T_J = 25°C		1.3	2.2	3.3	A
	V	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C/
				+25°C ≤ T_J ≤ 150°C			0.3	V_{OUT}

μA7808C

ELECTRICAL CHARACTERISTICS: V_{IN} = 14 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

CHARACTERISTICS		CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	80	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	80	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	160	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	80	mV
Output Voltage		10.5 V ≤ V_{IN} ≤ 23 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	10.5 V ≤ V_{IN} ≤ 25 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10Hz, ≤ f ≤ 100 kHz			52		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		56	72		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			16		mΩ
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			450		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.8		mV/°C

All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

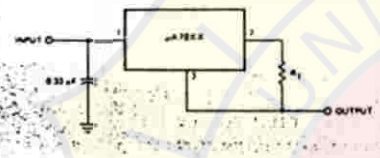
TYPICAL APPLICATIONS

NOTES:
1) To specify an output voltage, substitute voltage value for "XX".
2) Although no output capacitor is needed for stability, it does improve transient response.
3) Required if regulator is located an appreciable distance from power supply filter.

$$V_{OUT} = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_Q R_2$$

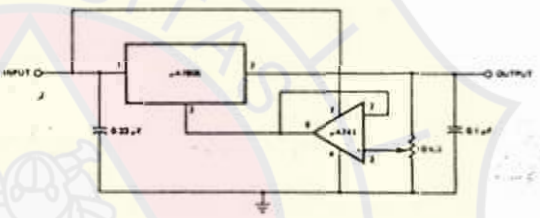
FIXED OUTPUT REGULATOR

CIRCUIT FOR INCREASING OUTPUT VOLTAGE



$$\text{Output Current} = \frac{V_{OUT}}{R_1}$$

CURRENT REGULATOR



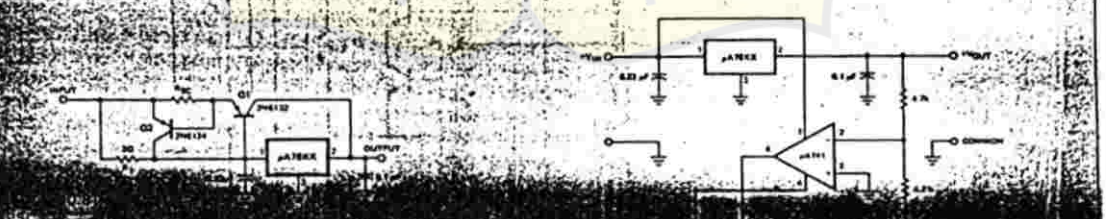
ADJUSTABLE OUTPUT REGULATOR, 7 to 30 VOLTS

$$\beta(Q1) > \frac{I_{OUT(MAX)}}{I_{REG\ (MAX)}}$$

$$R_1 = \frac{0.9 - \beta(Q1)\, V_{BE(Q1)}}{I_{REG} \times I_{REG(MAX)}(\beta+1) - I_{OUT(MAX)}}$$

0.5 TO 10 V REGULATOR

HIGH CURRENT VOLTAGE REGULATOR

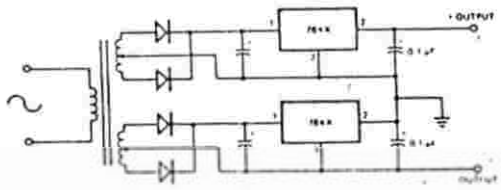


$$R_1 = \frac{V_{BE\ (Q1)}}{I_{REG(MAX)}(\beta+1) - I_{OUT(MAX)}}$$

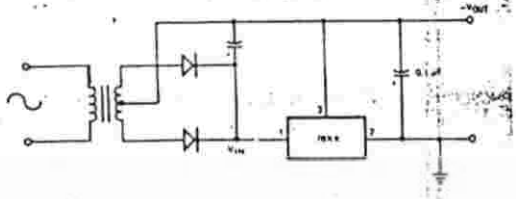
HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED

TRACKING VOLTAGE REGULATOR

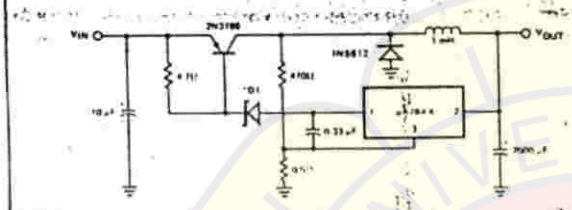
TYPICAL APPLICATIONS (Cont'd)



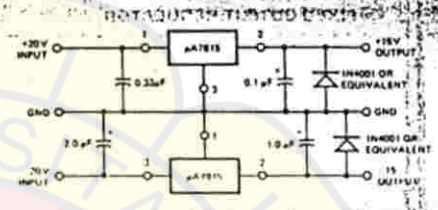
POSITIVE AND NEGATIVE REGULATOR



NEGATIVE OUTPUT VOLTAGE CIRCUIT



SWITCHING REGULATOR



DUAL SUPPLY OPERATIONAL AMPLIFIER SUPPLY (±15 V @ 1.0 A)

HIGH INPUT VOLTAGE CIRCUITS