BAB VI

KESIMPULAN

Setelah dilakukan penguji cobaan pada perangkat keras dari EPROM dengan menggunakan *MODE MINIMUM*, maka dapat diambil kesimpulan sebagai berikut :

- Sistem minimum ini bisa dipakai dalam berbagai hal instrumen elektronika, tetapi ada hal yang perlu diperhatikan sebelum merancang instrumen tersebut, pertama yaitu pertimbangan masalah kerumitan instrumen, jika memang instrumen tersebut masih bisa direalisasikan (secara mudah) dengan sistem biasa maka dibawah ini diterangkan sebagai pegangan untuk membuat suatu instrumen yang menggunakan μP.
  a. Dengan sistem biasa terlalu rumit untuk dilaksanakan.
  b. Instrumen yang akan kita buat dalam suatu saat perlu perubahan sedikit-sedikit.
  c. Instrumen yang akan dibuat diperlukan pengembangan ke arah penyempurnaan.
  d. Masalah waktu merupakan pembatasan akan respon yang harus dipenuhi oleh instrumen tersebut.
  e. Faktor ekonomis dan lain-lain.

Dalam software diperlukan kecermatan dan ketelitian untuk merealisasikan dan hal ini tergantung dari tingkat intelgensi pemrogram serta pengalaman dan latar belakang

pendidikan dan lain-lain. Untuk pengecekan sebuah program dapat menggunakan bahasa assembler misalnya MPF (Mikroprofesor), atau yang lainnya.

DAFTAR PUSTAKA

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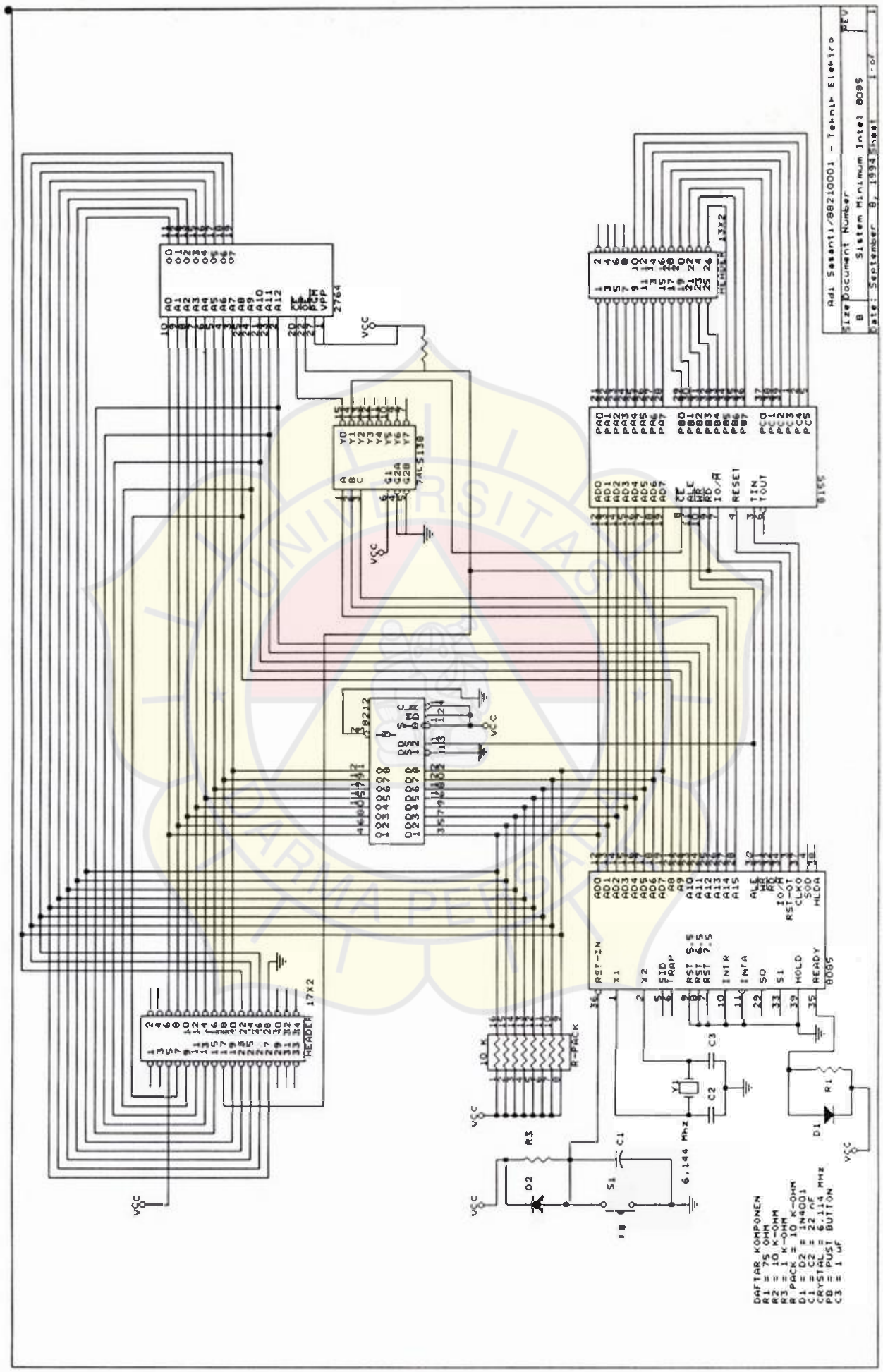
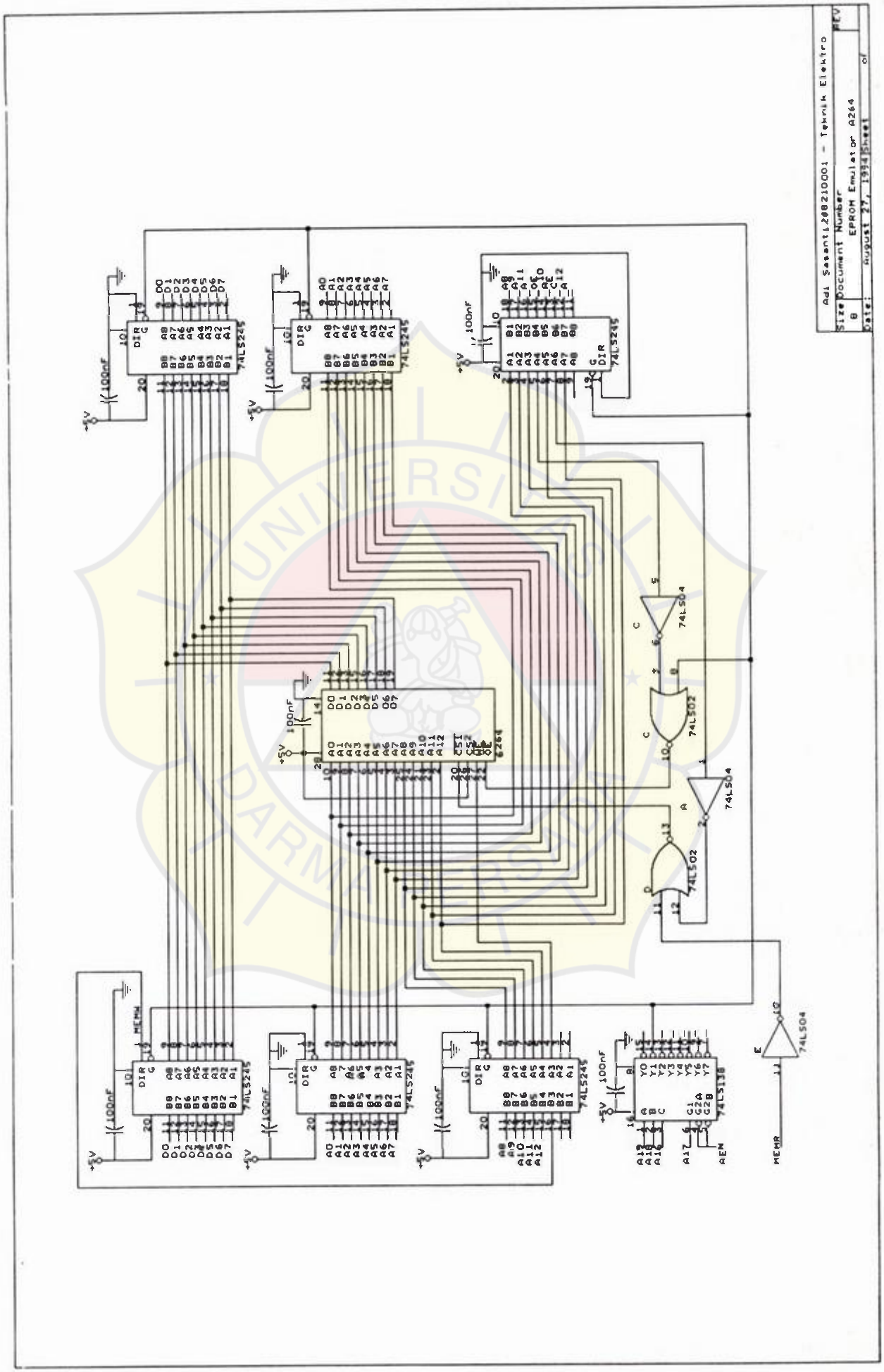
2. Short, Kenneth L., "*Microprocessors and Programmed Logic*" Prentice Hall International, Inc, New York, 1974.
3. Lubis, Edward P., "*Elektron Edisi 36*", Institut Teknologi Bandung.
4. Miller, Alan R., "*Pemrograman Bahasa Assembly pada DOS* ", Alih bahasa : Drs. Rudy Sujanto, Indomicros, 1990.
5. I B M, "*IBM-PC Technical Reference Manual*" , Boca Raton, 1983.

LAMPIRAN 1


Adi Sasanti/98210001 - Teknik Elektro
Size: B
Document Number
Sistem Minimum Intel 8085
Date: September 8, 1994
DAFTAR KOMPONEN
R1 = 75 OHM
R2 = 10 K-OHM
R3 = 1 K-OHM
R PACK = 10 K-OHM
D1 = D2 = 1N4001
C1 = C2 = 22 nF
CRYSTAL = 6.144 MHz
PB = PUSH BUTTON
C3 = 1 uF

LAMPIRAN 2


Adi Susanto|20821001 - Teknik Elektro
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B EPROM Emulator A264
Date: August 27, 1994 Sheet of
74LS245
74LS04
74LS02
74LS138
6264
100nF
+5V
MEMR
AEN

LAMPIRAN 3

PROGRAM : LED.ASM
NAMA : ADI SASANTI
NIM : 88210001
JURUSAN : TEKNIK ELEKTRO

```
0000                            ORG 00H
0000 00                         NOP
0001 00                         NOP
0002 00                         NOP

0003 31FE20     ALAMAT:         LXI  SP,20FEH
0006 210020                     LXI  H,2000H

0020            CONTROL:        EQU  20H
0021            PORT_A          EQU  21M
0022            PORT_B          EQU  22M
0009 3E0F       INIT:           MVI  A,0FH
000B D320                       OUT  CONTROL

000D 3E01       MULAI:          MVI  A,01H
000F 07         LOOP:           RLC
0010 D321                       OUT  PORT_A
0012 D322                       OUT  PORT_B
0016 CD1C00                     CALL DELAY
0019 C30F00                     JMP  LOOP

0010 06FF       DELAY:          MVI  B,0FFH

001E 0EFF       LOOP1:          MVI  C,0FFH
0020 0D         LOOP2:          DCR  C
0021 C22000                     JNZ  LOOP2
0024 05                         DCR  B
0025 C21E00                     JNZ  LOOP1
0028 C9                         RET
0000                            END
```

LAMPIRAN 4

Foto Rangkaian Minimum 8085 & LED

Foto Keseluruhan Alat

intel

8085AH/8085AH-2/8085AH-1
8-BIT HMOS MICROPROCESSORS

- Single +5V Power Supply with 10% Voltage Margins
- 3MHz, 5MHz and 6 MHz Selections Available
- 20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz
- 1.3 μs Instruction Cycle (8085AH); 0.8 μs(8085AH-2); 0.67 μs (8085AH-1)
- 100% Compatible with 8085A
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8085AH is a complete 8 bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's (8085AH (CPU), 8156H (RAM/IO) and 8355/8755A (ROM/PROM/IO)) while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085AH.

The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155H/8156H/8355/8755A memory products allow a direct interface with the 8085AH.

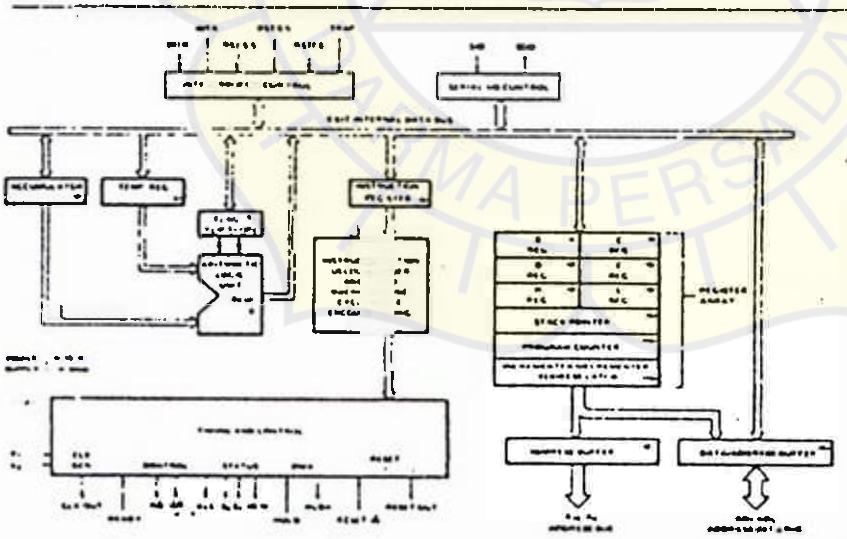


Figure 1. 8085AH CPU Functional Block Diagram

Figure 2. 8085AH Pin Configuration

intel

8155H/8156H/8155H-2/8156H-2 2048-BIT STATIC HMOS RAM WITH I/O PORTS AND TIMER

- Single +5V Power Supply with 10% Voltage Margins
- 30% Lower Power Consumption than the 8155 and 8156
- 100% Compatible with 8155 and 8156
- 256 Word x 8 Bits
- Completely Static Operation
- Internal Address Latch
- 2Programmable 8-Bit I/O Ports
- 1Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Compatible with 8085AH, 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with a 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085AH-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

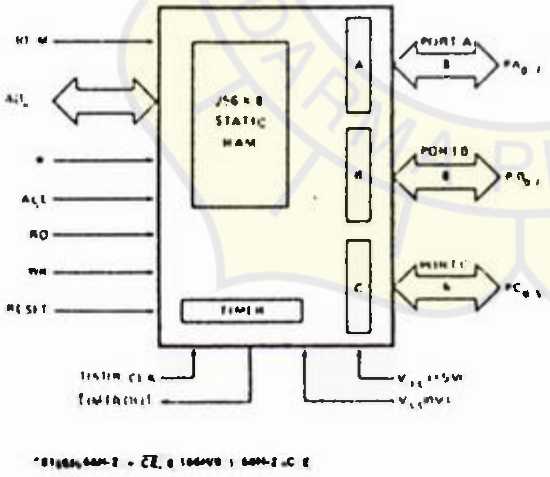


Figure 1. Block Diagram

Figure 2. Pin Configuration

intel

8212
8-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25mA Max.
- Three State Outputs
- Outputs Sink 15mA
- 3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

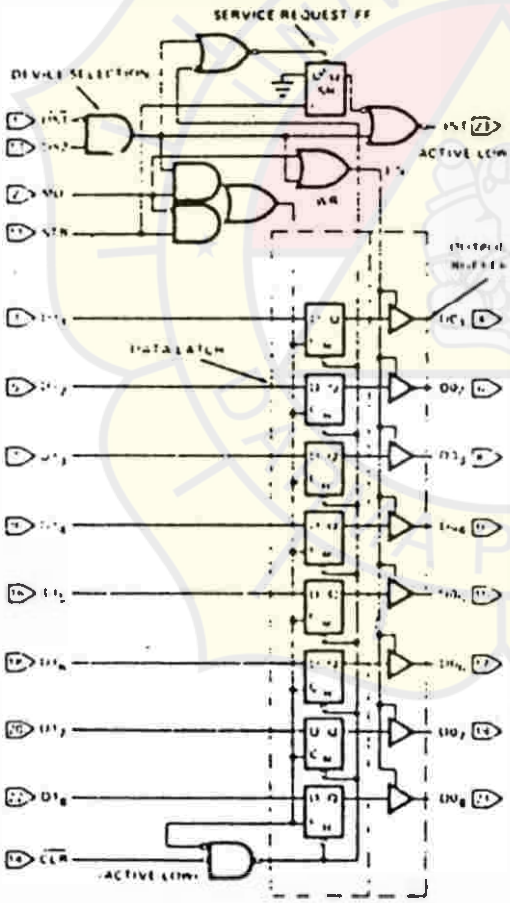


Figure 1. Logic Diagram

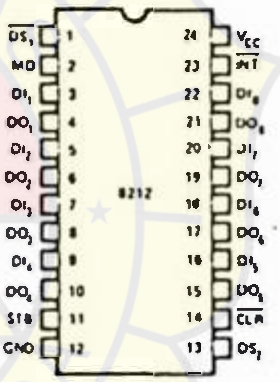


Figure 2. Pin Configuration

intel

2764
(8K x 8) UV ERASABLE PROM

- 200 ns (2764-2) Maximum Access Time... HMOS*-E Technology
- Compatible to high speed 8mHz 8086-2 MPU... Zero WAIT State
- Two Line Control
- Pin Compatible to 2732A EPROM
- Industry Standard Pinout... JEDEC Approved
- Low Standby Current...35mA Max.

The Intel® 2764 is a 5V only 65,536 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 2764 access time is 250ns with speed selection available at 200ns. The access time is compatible to high performance microprocessors, such as Intel's 8mHz 8086-2. In these systems, the 2764 allows the microprocessor to operate without the addition of WAIT states.

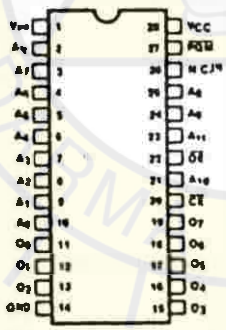
An important 2764 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 2764 has a standby mode which reduces the power dissipation without increasing access time. The active current is 150mA, while the standby current is only 35mA, a 75% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The 2764 is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

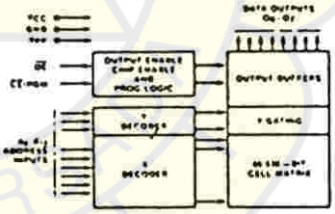
2732A PIN CONFIGURATION

2764 PIN CONFIGURATION



*For total compatibility from 27 32A provide a trace to pin 26

BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.(1)	NO CONNECT

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	x	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	x	x	V_{PP}	V_{CC}	High Z

x can be either V_{IL} or V_{IH}

*HMOS is a patented process of Intel Corporation.

Logic Products

74LS138, S138
Decoders/Demultiplexers

1-Of-8 Decoder/Demultiplexer
Product Specification

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{0}$–$\overline{7}$). The device features three Enable inputs: two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS138	20ns	6.3mA
74S138	[illegible]	49mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74S138N, N74LS138N
Plastic SO	N74LS138D, N74S138D

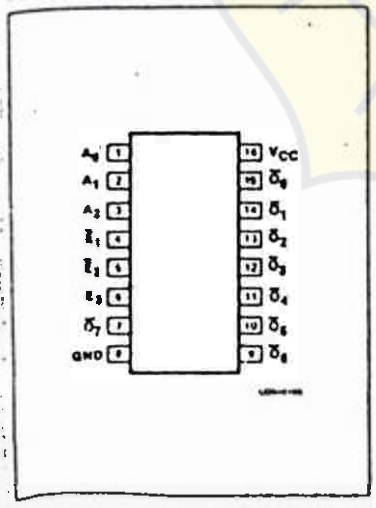
NOTE:
For information regarding devices processed to Military Specifications see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

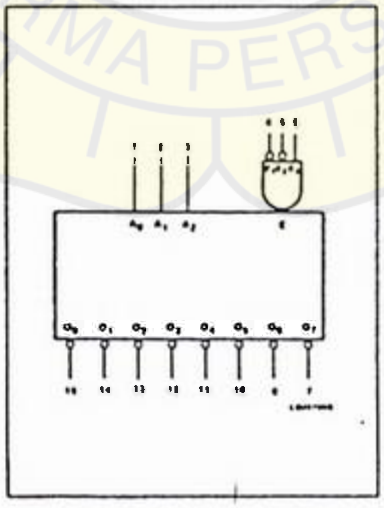
PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE:
Where a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

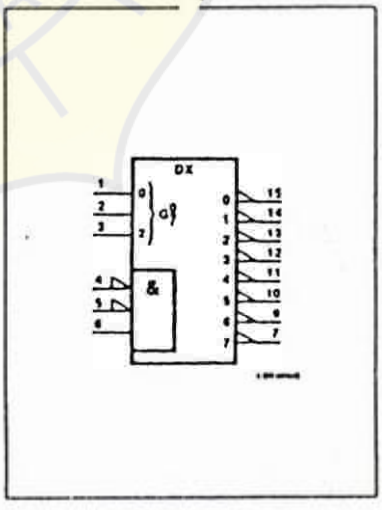
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



74LS245
Transceiver

Octal Transceiver (3-State)
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs

DESCRIPTION

The 'LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All data inputs have hysteresis built in to minimize AC noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS245	8ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS245N
Plastic SOL-20	N74LS245D

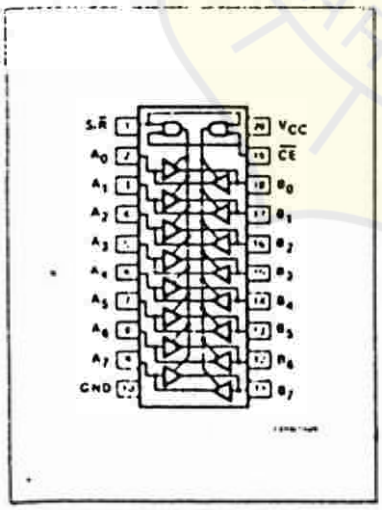
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

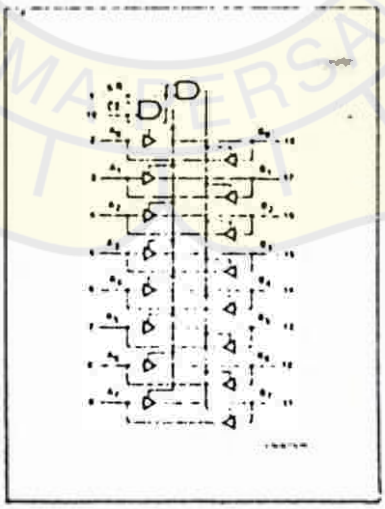
PINS	DESCRIPTION	74LS
All	Inputs	1L Sul
All	Outputs	30L Sul

NOTE:
Where a 74LS unit load (L Sul) is 20μA I_{IH} and -0.4mA I_{IL}

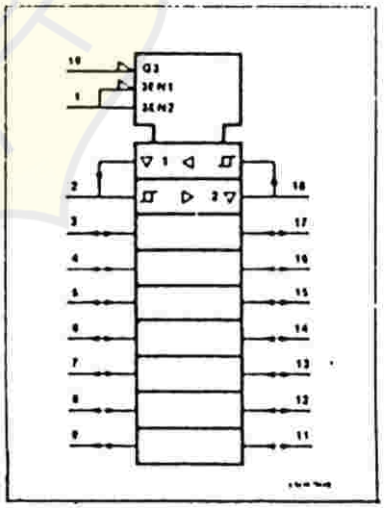
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Logic Products

7402, LS02, S02
Gates

Quad Two-Input NOR Gate
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7402	10ns	11mA
74LS02	10ns	2.2mA
74S02	3.5ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7402N, N74LS02N, N74S02N
Plastic SO	N74LS02D, N74S02D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

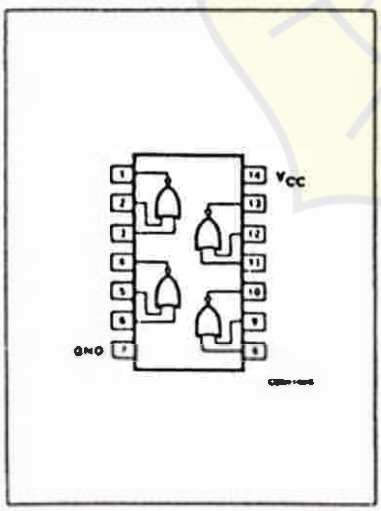
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

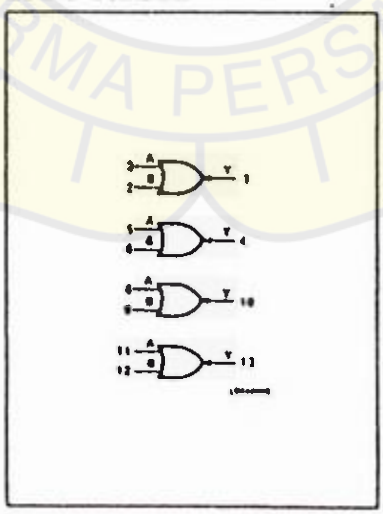
PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

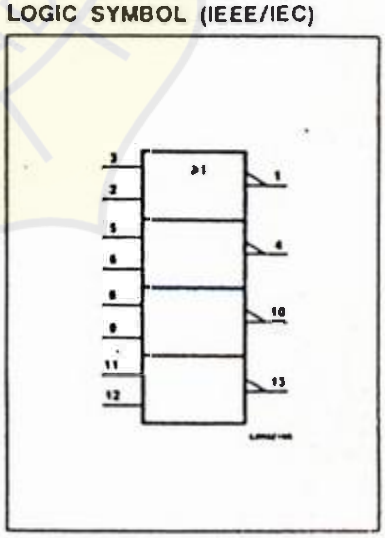
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



7404, LS04, S04
Inverters

Hex Inverter
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7404	10ns	12mA
74LS04	9.5ns	2.4mA
74S04	3ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7404N, N74LS04N, N74S04N
Plastic SO	N74LS04D, N74S04D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

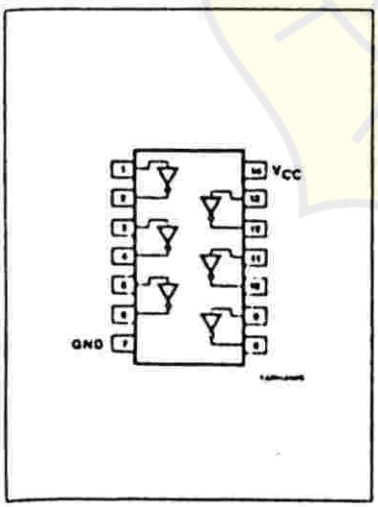
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

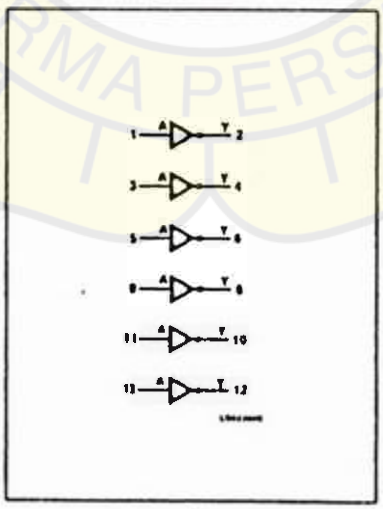
PINS	DESCRIPTION	74	74S	74LS
A	Input	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40 µA I_{IH} and −1.6mA I_{IL}, a 74S unit load (Sul) is 50µA I_{IH} and −2.0mA I_{IL}, and 74LS unit load (LSul) is 20µA I_{IH} and −0.4mA I_{IL}.

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)