BAB V

KESIMPULAN

Kesimpulan yang dapat diambil setelah mengerjakan tugas akhir ini adalah sebagai berikut :

a. Rancangan modulator 8-QAM dibentuk oleh 3 bit masukan dan menghasilkan kombinasi 4 beda Fasa dan 2 level amplitudo berbeda, yang membentuk 8 simbol sinyal

b. Input data biner masukan pada modulator 8-QAM menghasilkan 8 kombinasi yang terbagi menjadi 3 bit simbol yaitu 000,001,010,011,100,101,110,111 pada setiap 1 perioda gelombang signal pembawa.

c. Modulator 8-QAM yang dirancang dan setelah melalui pengukuran di laboratorium sudah bekerja sesuai dengan apa yang diharapkan di mana sinyal keluarannya menghasilkan 8 titik konstelasi QAM

LAMPIRAN 1

DATA SHEET

MC1496 *Balance Modulator*

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MC1496 Balanced Modulator

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APPLICATION NOTE

INTRODUCTION

The ON Semiconductor MC1496 monolithic balanced modulator makes an excellent building block for high frequency communications equipment.

The device functions as a broadband, double sideband suppressed carrier balanced modulator without a requirement for transformers or tuned circuits. In addition to its basic application as a balanced modulator/demodulator, the device offers excellent performance as an SSB product detector, AM modulator/detector, FM detector, mixer, frequency doubler, phase detector, and more.

The article consists of a general description of the MC1496, its gain equations, biasing information, and circuits illustrating typical applications. It is followed by an appendix containing a detailed mathematical ac and dc analysis of the device.

Many readers may find that one of the circuits described in the article will fill the needs of their application. However, it is impossible to show typical circuits for every possible requirement, and the detailed analysis given in the appendix will assist the designer in developing an optimum circuit for any application within the basic capabilities of the MC1496.

MC1496 General Description

Figure 1 shows a schematic diagram of the MC1496. For purposes of the analysis, the following conventional assumptions have been made for simplification: (1) Devices of similar geometry within a monolithic chip are assumed identical and matched where necessary, and (2) transistor base currents are ignored with respect to the magnitude of collector currents; therefore, collector and emitter currents are assumed equal.

Referring to Figures 1 and 2, the MC1496 consists of differential amplifier Q5-Q6 driving a dual differential amplifier composed of transistors Q1, Q2, Q3 and Q4. Transistors Q7 and Q8 and associated bias circuitry form constant current sources for the lower differential amplifier Q5-Q6.

The analysis of operation of the MC1496 is based on the ability of the device to deliver an output which is proportional to the product of the input voltages V_X and V_Y. This holds true when the magnitudes of V_X and V_Y are maintained within the limits of linear operation of the three differential amplifiers in the device. Expressed mathematically, the output voltage (actually output current, which is converted to an output voltage by an external load resistance), V_O is given by

$$V_O = KV_X V_Y \quad (1)$$

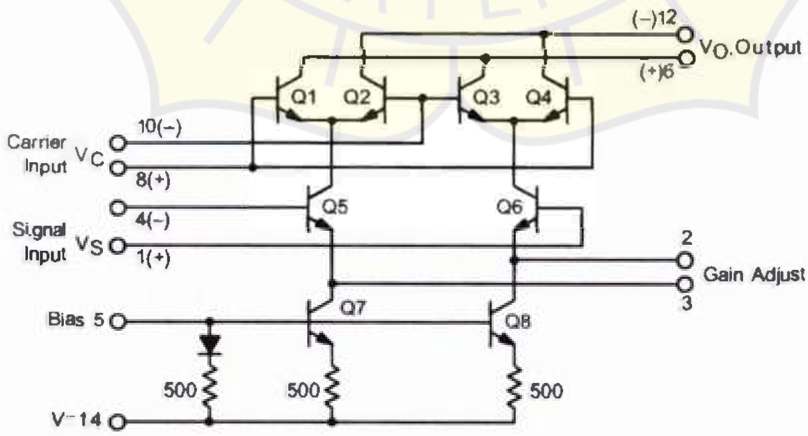

Figure 1. MC1496 Schematic

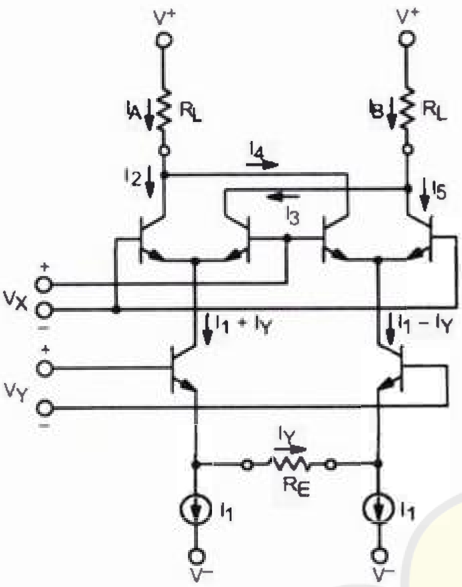

Figure 2. Analysis Model

where the constant K may be adjusted by choice of external components. A detailed description of how the MC1496 circuit configuration performs the basic function of multiplication as expressed by Equation (1) is contained in the references.

An example of a four–quadrant multiplier utilizing these principles is the ON Semiconductor MC1595, which has been described in a previous article.[4] The MC1595 multiplier contains the basic circuit configuration of the MC1496 plus additional circuitry which results in linear multiplier operation over a large input voltage range. However, the less complex MC1496 has higher frequency response, greater versatility and is less expensive than the MC1595. For these reasons the MC1496 is preferred in many communications applications such as those to be described later in this note.

Device Operation

The most common mode of operation of the MC1496 consists of applying a high level input signal to the dual differential amplifiers, Q1, Q2, Q3, and Q4, (carrier input port) and a low level input signal to the lower differential amplifier, Q5 and Q6, (modulating signal input port). This results in saturated switching operation of carrier dual differential amplifiers, and linear operation of the modulating differential amplifier.

The resulting output signal contains only the sum and difference frequency components and amplitude information of the modulating signal. This is the desired condition for the majority of the applications of the MC1496.

Saturated operation of the carrier–input dual differential amplifiers also generates harmonics (which may be predicted by Fourier analysis, see Appendix). Reducing the carrier input amplitude to its linear range greatly reduces these harmonics in the output signal. However, it has the disadvantages of reducing device gain and causing the output signal to contain carrier signal amplitude variations.

The carrier input differential amplifiers have no emitter degeneration. Therefore, the carrier input levels for linear and saturated operation are readily calculated. (See Appendix.) The crossover point is in the vicinity of 15–20 mV rms, with linear operation below this level and saturated operation above it.

The modulating signal differential amplifier has its emitters brought out to pins 2 and 3. This permits the designer to select his own value of emitter degeneration resistance and thereby tailor the linear dynamic range of the modulating–signal input port to a particular requirement. The resistor also determines device gain.

The approximate maximum level of modulating signal input for linear operation is given by the expression:

$$V_m(\text{peak}) = I_1 R_E \tag{2}$$

where R_E = resistance between pins 2 and 3, and I_1 refers to the notation in the analysis model shown in Figure 2. Since base currents were assumed to be zero and transistors identical,

$$I_1 = I_5 \tag{3}$$

where I_5 = current flowing into pin 5. Therefore, Equation (2) becomes

$$V_y(\text{peak}) = I_5 R_E \tag{4}$$

Device voltage gain (single ended output with respect to modulating signal input) is given by the expression (also see Appendix):

$$A_V = \frac{R_L}{R_E} f(m) \tag{5}$$

where

$$f(m) = \left[\frac{e^{-m} - e^{m}}{(1 + e^{m})(1 + e^{-m})}\right]$$

$$m = \frac{V_X}{\frac{kT}{q}}$$

f(m) may be approximated for the two general cases of high and low level carrier operation, resulting in the following gain expressions: High level case (V_X > 100 mV peak):

$$f(m) \approx 1 \tag{6}$$

therefore,

$$|A_V| \approx \frac{R_L}{R_E} \tag{7}$$

The low–level case (V_X < 50 mV peak) is given by:

$$f(m) \approx \frac{-m}{2} \tag{8}$$

therefore,

$$|A_V| \approx \frac{R_L m}{2R_E} \tag{9}$$

The foregoing expressions assume the condition $R_E \gg r_e$, where r_e is the dynamic emitter resistance of transistors Q5 and Q6. When I_1 = 1 mA, r_e is approximately 26 ohms at room temperature.

There are numerous applications where it is desirable to set R_E equal to some low value or zero. For this condition, Equations (7) and (9) can be expanded to the more general form:

high level V_X:

$$|A_V| \approx \frac{R_L}{R_E + 2r_e} \tag{10}$$

low level V_X:

$$|A_V| \approx \frac{R_{Lm}}{2(R_E + 2r_e)} \tag{11}$$

Equations (10) and (11) summarize the single ended conversion voltage gains of the MC1496 with a dc input voltage (V_X) at the carrier port. Operation with a differential output would increase the gains by 6 dB.

Equations (10) and (11) may be combined with Equations (26) and (29) in the Appendix to compute the conversion gain of the MC1496 operating as a double sideband suppressed carrier modulator (ac carrier input).

For a high level carrier input signal, the expressions for output voltage and voltage gain become

$$V_O = \frac{R_L V_y}{R_E + 2r_e} \sum_{n=1}^{\infty} A_n[\cos(n\omega_x + \omega_y)t + \cos(n\omega_x - \omega_y)t] \tag{12}$$

where

$$A_n = \left[\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\right]$$

Solving Equation (12) for the sidebands around f_X (n= 1) yields:

$$V_O = \frac{R_L V_y}{R_E + 2r_e}(0.637)[\cos(\omega_x + \omega_y)t + \cos(\omega_x - \omega_y)t] \tag{13}$$

Equation (13) may be further simplified to give the voltage gain for the amplitude of each fundamental sideband:

$$\frac{V_O}{V_y} = A_v = \frac{0.637 R_L}{R_E + 2r_e} \tag{14}$$

For the low level V_X case:

$$V_O = \frac{-R_L V_y(\cos\omega_y)t\left[\frac{V_x(\cos\omega_x)t}{kT/q}\right]}{2(R_E + 2r_e)} \tag{15}$$

$$V_O = \frac{-R_L V_y V_x[\cos(\omega_x + \omega_y)t + \cos(\omega_x - \omega_y)t]}{4\left(\frac{kT}{q}\right)(R_E + 2r_e)} \tag{16}$$

And the voltage gain for each sideband becomes:

$$\left|V_O\right| = |A_v| = \frac{R_L V_x(\text{rms})}{2\sqrt{2}\left(\frac{kT}{q}\right)(R_E + 2r_e)} \tag{17}$$

Equations (14) and (17) summarize the single ended conversion voltage gains of the MC1496 for low and high level ac carrier inputs. Note that these gain expressions are calculated for the output amplitude of each of the two desired sidebands. The composite output signal consists of the sum of these two sidebands in the low level case and in the high level case it is the sum of the sidebands of the carrier and all the odd numbered harmonics of the carrier.

Laboratory gain measurements have shown good correlation with Equations (10), (11), (14) and (17).

DC Bias

A significant portion of the DC bias circuitry for the MC1496 must be supplied externally. While this has the disadvantage of requiring several external components, it has the advantage of versatility. The MC1496 may be operated with either single or dual power supplies at practically any supply voltage(s) a semiconductor system has available. Further, the external load and emitter resistors provide the designer with complete freedom in setting device gain.

The DC bias design procedure consists of setting bias currents and 4 bias voltage levels, which not exceeding absolute maximum voltage, current, and dissipation ratings.

The current levels in the MC1496 are set by controlling I_5 (subscripts refer to pin numbers). For bias current design the following assumption may be made:

$$I_5 = I_6 = I_{12} = \frac{I_{14}}{3}$$

Since base currents may be neglected, I_5 flows through a forward biased diode and a 500 Ω resistor to pin 14.

When pin 14 is grounded, I_5 is most conveniently adjusted by driving pin 5 from a current source.

When pin 14 is connected to a negative supply, I_5 may be set by connecting a resistor from pin 5 to ground (R5). The value of R5 may be computed from the following expression:

$$R_5 = \frac{|V_{14}| - \phi}{I_5} - 500\ \Omega \tag{18}$$

where ϕ = the diode forward voltage, or about 0.75 Vdc at T_A = 25°C.

The absolute maximum rating for I_5 is 10 mA.

For all applications described in the article, bias current I_5 has been set at 1 mA. The MC1496 has been characterized at this bias current and it is the recommended current unless there is a conflict with power dissipation requirements.

The 4 bias voltage levels that must be set up externally are:

- pins 6 and 12 most positive;
- pins 8 and 10 next most positive;
- pins 1 and 4 next most positive;
- pin 14 most negative.

The intermediate voltage levels may be provided by a voltage divider(s) or any other convenient source such as ground in a dual power supply system.

It is recommended that the voltage divider be designed for a minimum current of 1 mA. Then I_1, I_4, I_7, and I_8 need not be considered in the divider design as they are transistor base currents.

Guidelines for setting up the bias voltage levels include maintaining at least 2 volts collector-base bias on all

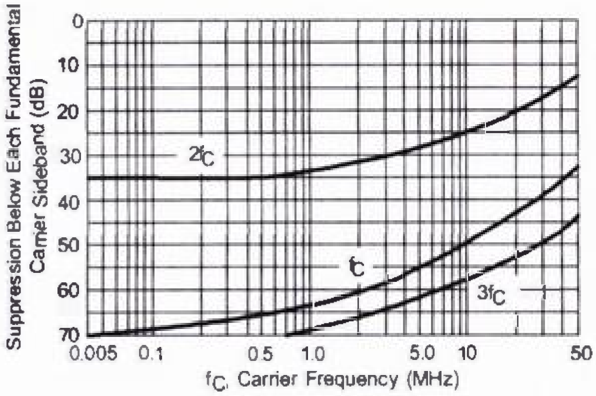

Figure 4. Balanced Modulator Carrier Suppression versus Frequency

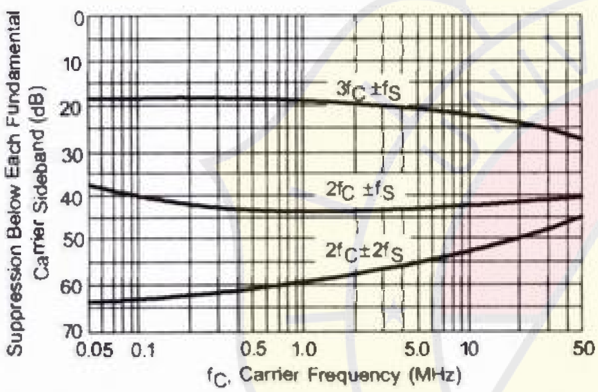

Figure 5. Balanced Modulator Suppression of Carrier Harmonic Sidebands versus Carrier Frequency

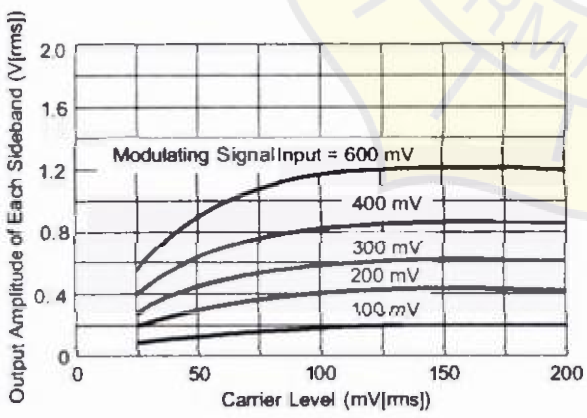

Figure 6. Balanced Modulator Sideband Output versus Carrier and Modulating Signal Inputs. Single Ended Operation.

Table 1. Suppression in dB of Spurious Outputs Below Each Desired Sideband ($f_C \pm f_S$) for High and Low Level Carrier Injection Voltages

	f_C	$2f_C$	$3f_C$	$2f_C \pm f_S$	$3f_C \pm f_S$
High Level Carrier Input 60 mV(rms)	66 dB	35 dB	70 dB	43 dB	19 dB
Low Level Carrier Input 10 mV(rms)	66 dB	45dB	70 dB	53 dB	46 dB

Carrier Frequency = 500 kHz.
Modulating Signal = 1.0 kHz at 300 mV(rms).
Circuit of Figure 3.

Spurious levels during low level operation are so low that they are affected significantly by the special purity of the carrier input signal. For example, initial readings for Table 1 were taken with a carrier signal generator which has second and third harmonics 42 and 45 dB below the fundamental, respectively. Additional filtering of the carrier input signal was required to measure the true second and third carrier–harmonic suppression of the MC1496.

The decision to operate with a low or high level carrier input would of course depend on the application. For a typical filter–type SSB generator, the filter would remove all spurious outputs except some spurious sidebands of the carrier. For this reason operation with a high level carrier would probably be selected to maximize gain and insure that the desired sideband does not contain any spurious amplitude variations present on the carrier input signal.

On the other hand, in a low frequency broadband balanced modulator spurious outputs at any frequency may be undesirable and low level carrier operation may be the best choice.

Good carrier suppression over a wide temperature range requires low dc resistances between the bases of the lower differential amplifier (pins 1 and 4) and ground. It is recommended that the values of these resistors not be increased significantly higher than the 51 ohms utilized in the circuit shown in Figure 3 in applications where carrier suppression is important over full operating temperature range of –40°C to +125°C. Where operation is to be over a limited temperature range, resistance values of up to the low kilohm range may be used.

Amplitude Modulator

The MC1496 balanced modulator circuit shown in Figure 3 will function as an amplitude modulator with just one minor modification. All that is necessary is to unbalance the carrier null to insert the proper amount of carrier into the output signal. However, the null circuitry used for balanced modulator operation does not provide sufficient adjustment range and must be modified. The resulting amplitude modulator is shown in Figure 7. This modulator will provide excellent modulation at any percentage from zero to greater than 100 percent.

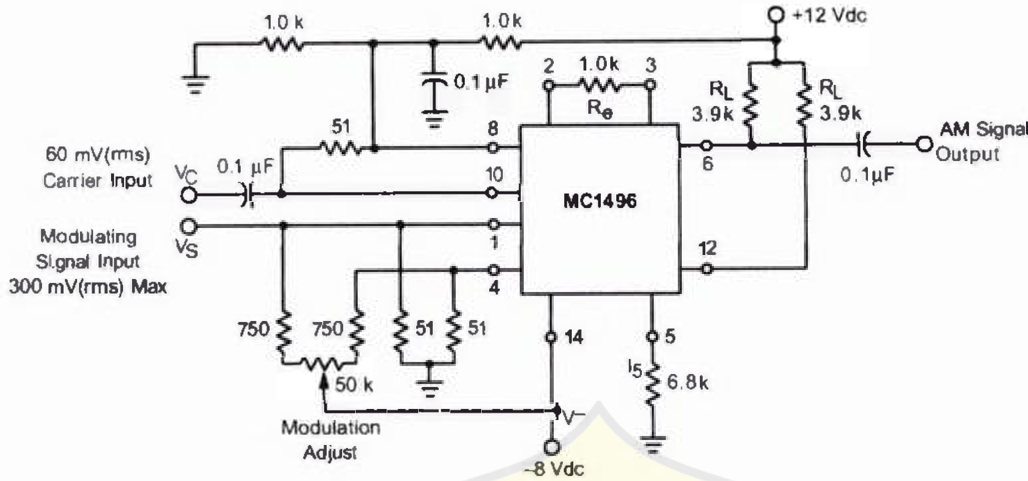

Figure 7. Amplitude Modulator

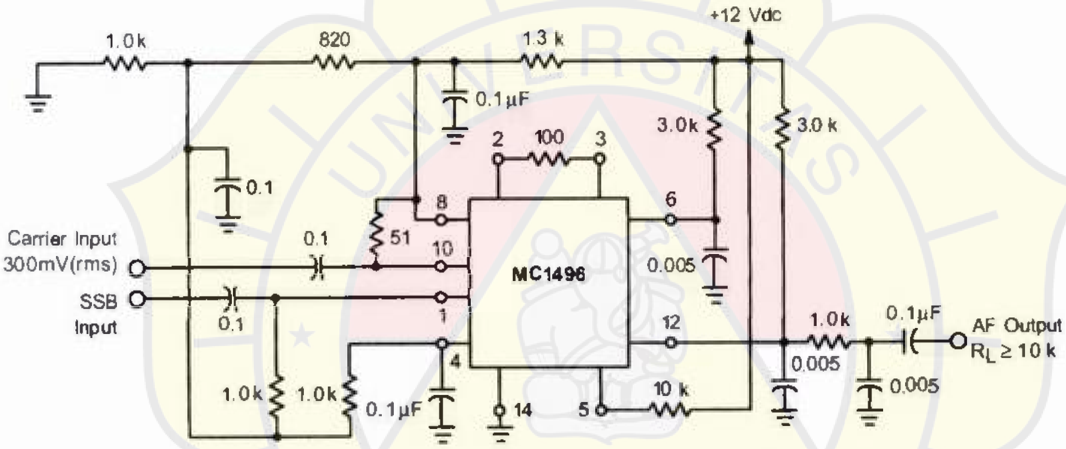

Figure 8. Product Detector +12 Vdc Single Supply

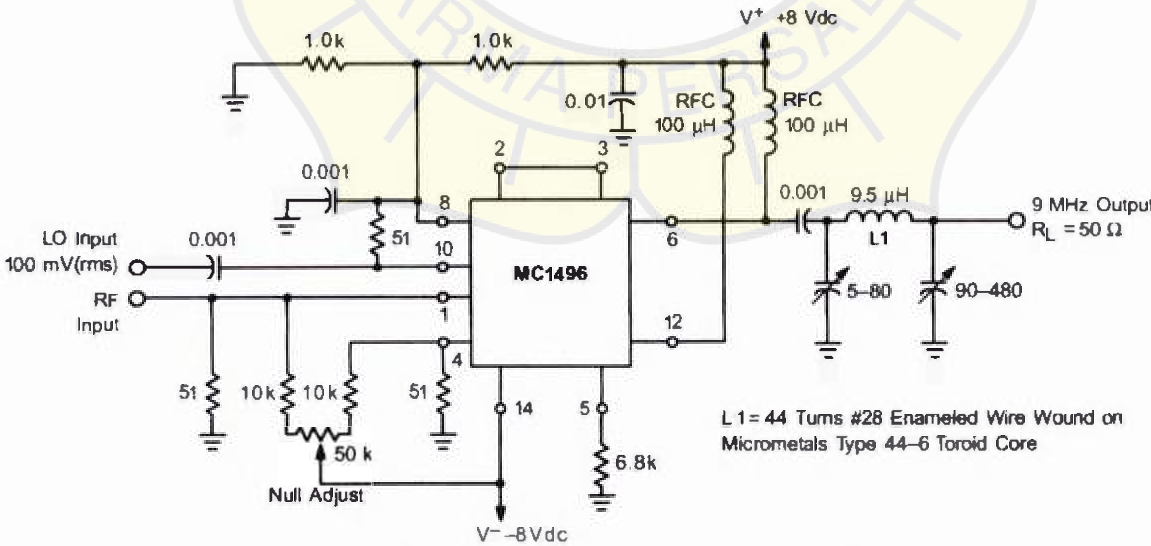

Figure 9. Double Balanced Mixer, Broadband Inputs, 9 MHz Tuned Output

Product Detector

Figure 8 shows the MC1496 in an SSB product detector configuration. For this application, all frequencies except the desired demodulated audio are in the RF spectrum and can be easily filtered in the output. As a result, the carrier null adjustment need not be included.

Upper differential amplifiers Q1–Q2 and Q3–Q4 are again driven with a high level signal. Since carrier output level is not important in this application (carrier is filtered in the output) carrier input level is not critical. A high level carrier input is desirable to maximize gain of the detector and to remove any carrier amplitude variations from the output. The circuit of Figure 8 performs well with a carrier input level of 100 to 500 mV rms.

The modulated signal (single–sideband, suppressed carrier) input level to differential amplifier pair Q5–Q6 is maintained within the limits of linear operation. Excellent linearity and undistorted audio output may be achieved with an SSB input signal level range up to 100 mV rms. Again, no transformers or tuned circuits are required for excellent product detector performance from very low frequencies up to 100 MHz.

Another advantage of the MC1496 product detector is its high sensitivity. The sensitivity of the product detector shown in Figure 8 for a 9 MHz SSB signal input and a 10 dB signal plus noise to noise [(S + N)/N] ratio at the output is 3 microvolts. For a 20 dB (S + N)/N ratio audio output signal it is 9 microvolts.

For a 20 dB (S + N)/N ratio, demodulated audio output signal, a 9 MHz SSB input signal power of –101 dBm is required. As a result, when operated with an SSB receiver with a 50 ohm input impedance, a 0.5 microvolt RF input signal would require only 12 dB overall power gain from antenna input terminals to the MC1496 product detector.

Note also that dual outputs are available from the product detector, one from pin 6 and another from pin 12. One output can drive the receiver audio amplifiers while a separate output is available for the AGC system.

AM Detector

The product detector circuit of Figure 8 may also be used as an AM detector. The modulated signal is applied to the upper differential amplifiers while the carrier signal is applied to the lower differential amplifier.

Ideally, a constant amplitude carrier signal would be obtained by passing the modulated signal through a limiter ahead of the MC1496 carrier input terminals. However, if the upper input signal is at a high enough level (> 50 mV), its amplitude variations do not appear in the output signal. For this reason it is possible to use the product detector circuit shown in Figure 8 as an AM detector simply by applying the modulated signal to both inputs at a level of about 600 mV on modulation peaks without using a limiter ahead of the carrier input port. A small amount of distortion will be generated as the signal falls below 50 mV during modulation valleys, but it will probably not be significant in most applications. Advantages of the MC1496 AM detector include linear operation and the ability to have a detector stage with gain.

Mixer

Since the MC1496 generates an output signal consisting of the sum and difference frequencies of the two input signals only, it can also be used as a double balanced mixer.

Figure 9 shows the MC1496 used as a high frequency mixer with a broadband input and a tuned output at 9 MHz. The 3 dB bandwidth of the 9 MHz output tank is 450 kHz.

The local oscillator (LO) signal is injected at the upper input port with a level of 100 mV rms. The modulated signal is injected at the lower input port with a maximum level of about 15 mV rms. Note that for maximum conversion gain and sensitivity the external emitter resistance on the lower differential amplifier pair has been reduced to zero.

For a 30 MHz input signal and a 39 MHz LO, the mixer has a conversion gain of 13 dB and an input signal sensitivity of 7.5 microvolts for a 10 dB (S + N)/N ratio in the 9 MHz output signal. With a signal input level of 20 mV, the highest spurious output signal was at 78 MHz (2 f_{LO}) and it was more than 30 dB below the desired 9 MHz output. All other spurious outputs were more than 50 dB down.

As the input is broadband, the mixer may be operated at any HF and VHF input frequencies. The same circuit was operated with a 200 MHz input signal and a 209 MHz LO. At this frequency the circuit had 9 dB conversion gain and a 14microvolt sensitivity.

Greater conversion gains can be achieved by using tuned circuits with impedance matching on the signal input port. Since the input impedance of the lower input port is considerably higher than 50 ohms even with zero emitter resistance, most of the signal input power in the broadband configuration shown is being dissipated in the 50 ohm resistor at the input port.

The circuit shown has the advantage of a broadband input with simplicity and reasonable conversion gain. If greater conversion gain is desired, impedance matching at the signal input is recommended.

The input impedance at the signal input port is plotted in Figures 10 and 11. The output impedance is also shown in Figure 12. Both of these curves indicate the complex impedance versus frequency for single ended operation.

The nulling circuit permits nulling of the LO signal and results in a few dB additional LO suppression in the mixer output. The nulling circuitry (the two 10 kΩ resistors and 50 kΩ potentiometer) may be eliminated when operating with a tuned output in many applications where the combination of inherent device balance and the output tank provide sufficient LO suppression.

The tuned output tank may be replaced with a resistive load to form a broadband input and output doubly–balanced mixer. Magnitude of output load resistance becomes a simple matter of tradeoff between conversion gain and output signal bandwidth. As shown in Figure 12, the single ended output capacitance of the MC1496 at 9 MHz is typically 5 pF.

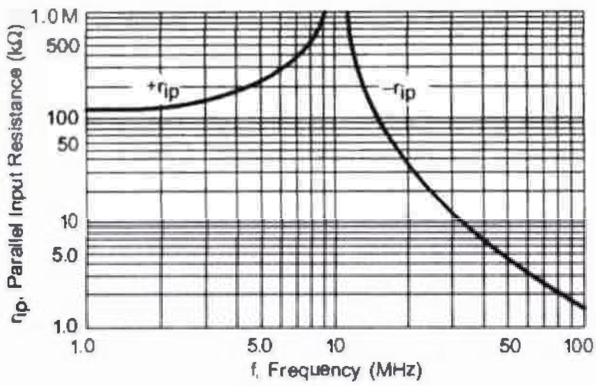

Figure 10. Signal–Port Parallel–Equivalent Input Resistance versus Frequency

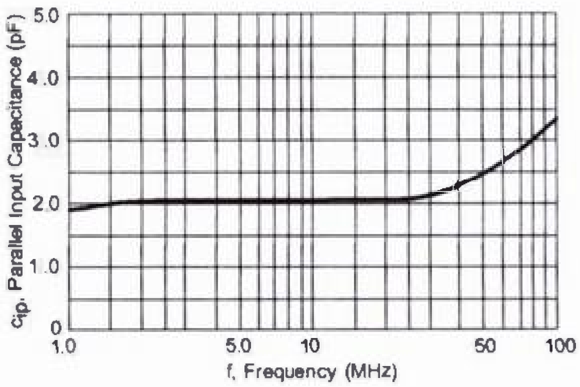

Figure 11. Signal–Port Parallel–Equivalent Input Capacitance versus Frequency

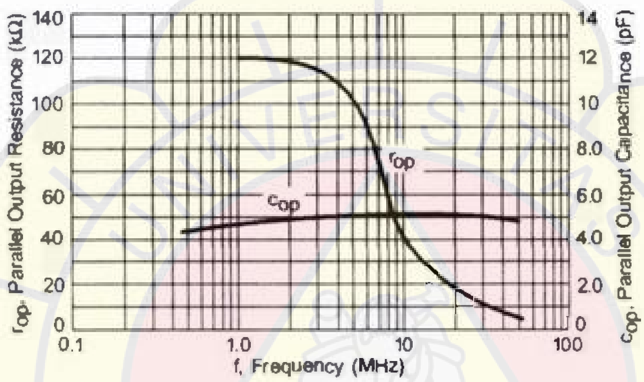

Figure 12. Single–Ended Output Impedance versus Frequency

With a 50 ohm output load, a 30 MHz input signal level of 20 mV, and 39 MHz LO signal level of 100 mV the conversion gain was −8.4 dB (loss). Isolation was 30 dB from input signal port to output port and 18 dB from LO signal port to output port.

Doubler

The MC1496 functions as a frequency doubler when the same signal is injected in both input ports. Since the output signal contains only $\omega_1 \pm \omega_2$ frequency components, there will be only a single output frequency at $2\omega_1$ when $\omega_1 = \omega_2$.

For operation as a broadband low frequency doubler, the balanced modulator circuit of Figure 3 need be modified only by adding ac coupling between the two input ports and reducing the lower differential amplifier emitter resistance between pins 2 and 3 to zero (tieing in 2 to pin 3). The latter modification increases the circuit sensitivity and doubler gain.

A low frequency doubler with these modifications is shown in Figure 13. This circuit will double in the audio and low frequency range below 1 MHz with all spurious outputs greater than 30 dB below the desired 2 f_{IN} output signal.

For optimum output signal spectral purity, both upper and lower differential amplifiers should be operated within their linear ranges. This corresponds to a maximum input signal level of 15 mV rms for the circuit shown in Figure 13.

If greater signal handling capability is desired the circuit may be modified by using a 1000 ohm resistance between pins 2 and 3 and a 10:1 voltage divider to reduce the input signal at the upper port to 1/10 the signal level at the lower port.

The MC1496 will also function very well as an RF doubler at frequencies up to and including UHF. Either a broadband or a tuned output configuration may be used.

Suppression of spurious outputs is not as good at VHF and UHF. However, in the broadband configuration, the desired doubled output is still the highest magnitude output signal when doubling from 200 to 400 MHz, where the spurious outputs are 7 dB or more below the 400 MHz output. Even at this frequency the MC1496 is still superior to a conventional transistor doubler before output filtering.

Figure 14 shows a 150 to 300 MHz doubler with output filtering. All spurious outputs are 20 dB or more below the desired 300 MHz output.

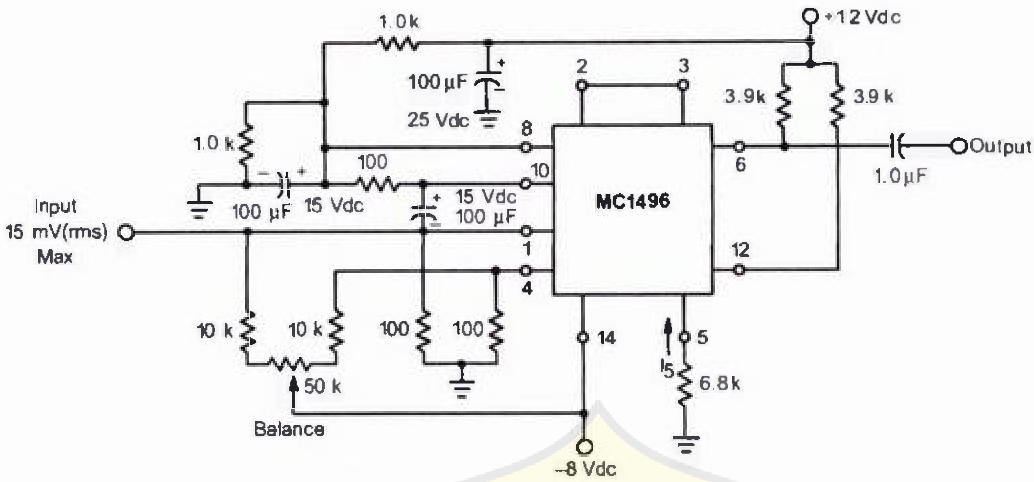

Figure 13. Low Frequency Doubler

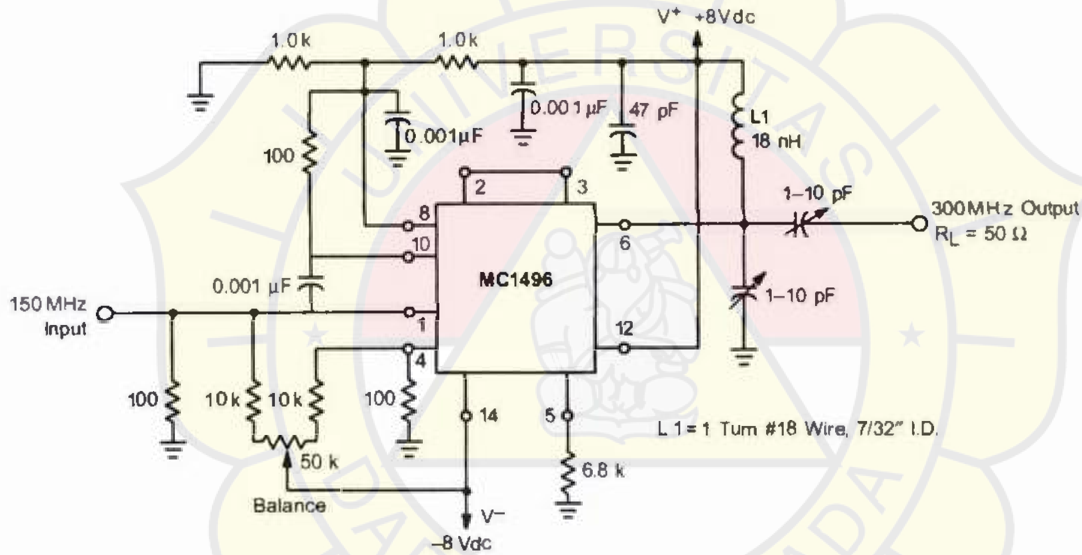

Figure 14. 150–300 MHz Doubler

FM Detector and Phase Detector

The MC1496 provides a dc output which is a function of the phase difference between two input signals of the same frequency, and can therefore be used as a phase detector. This characteristic can also be utilized to design an FM detector with the MC1496. All that is required is to provide a means by which the phase difference between the signals at the two input ports vary with the frequency of the FM signal.

Phase dependent FM detector operation can be explained by considering input and output currents for a high level signal at both input ports. These waveforms are shown in Figure 15 with inputs in phase at A and out of phase at B.

Since the output current is a constant times the product of the input currents, Figure 15 illustrates how a shift in phase between the two input signals causes a dc level shift in the output.

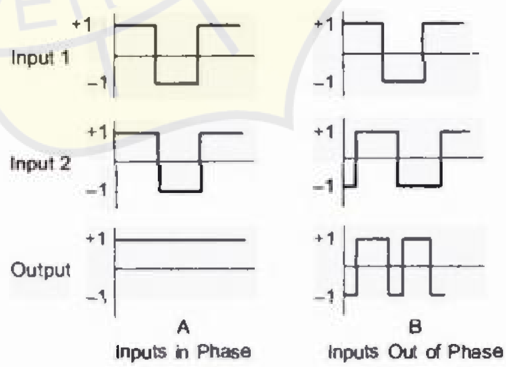

Figure 15. Phase Detector Waveforms, High Level Inputs

Summary

A number of applications of the MC1496 monolithic balanced modulator integrated circuit have been explored. The basic device characteristics of providing an output signal at the sum and difference of the two input frequencies with options on gain and amplitude characteristics will undoubtedly lead to numerous other applications not discussed in this article.

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APPENDIX

AC and DC Analysis

With reference in Figure 2 of the text, the following equations apply:

$$I_y = \frac{V_y}{R_E} \quad \text{(when } R_E >> r_e, \text{ the transistor dynamic emitter resistance.)} \tag{1A}$$

$$I_2 = \frac{I_1 + I_y}{1 + e^{\frac{V_x}{a}}}, \quad I_3 = \frac{I_1 + I_y}{1 + e^{\frac{-V_x}{a}}}, \quad I_4 = \frac{I_1 - I_y}{1 + e^{\frac{-V_x}{a}}}, \quad I_5 = \frac{I_1 - I_y}{1 + e^{\frac{V_x}{a}}} \tag{2A}$$

where

$$a = \frac{kT}{q} \tag{3A}$$

$$I_A = I_2 + I_4 = \frac{I_1 + I_y}{1 + e^m} + \frac{I_1 - I_y}{1 + e^{-m}}, \quad I_B = I_3 + I_5 = \frac{I_1 + I_y}{1 + e^{-m}} + \frac{I_1 - I_y}{1 + e^m} \tag{4A}$$

where

$$m = \frac{V_x}{a}$$

$$I_A - I_B = (I_1 + I_y)\left[\frac{1}{1 + e^m} - \frac{1}{1 + e^{-m}}\right] + (I_1 - I_y)\left[\frac{1}{1 + e^{-m}} - \frac{1}{1 + e^m}\right] \tag{5A}$$

$$= (I_1 + I_y)\left[\frac{1 + e^{-m} - 1 - e^m}{(1 + e^m)(1 + e^{-m})}\right] + (I_1 - I_y)\left[\frac{1 + e^m - 1 - e^{-m}}{(1 + e^{-m})(1 + e^m)}\right]$$

$$= \frac{(I_1 + I_y)(e^{-m} - e^m) + (I_1 - I_y)(e^m - e^{-m})}{(1 + e^m)(1 + e^{-m})}$$

$$= \frac{\left[\begin{matrix} I_1e^{-m} - I_1e^m + I_ye^{-m} - I_ye^m \\ I_1e^m - I_1e^{-m} - I_ye^m + I_ye^{-m} \end{matrix}\right]}{(1 + e^m)(1 + e^{-m})}$$

$$= \frac{2I_y(e^{-m} - e^m)}{(1 + e^m)(1 + e^{-m})}$$

$$\Delta V_O = (I_A - I_B)R_L \tag{6A}$$

$$= \frac{2I_yR_L(e^{-m} - e^m)}{(1 + e^m)(1 + e^{-m})}$$

But,

$$I_y = \frac{V_{in}}{R_E} \tag{7A}$$

Therefore,

$$\frac{\Delta V_O}{V_{in}} = \frac{2R_L}{R_E}\left[\frac{e^{-m} - e^m}{(1 + e^m)(1 + e^{-m})}\right] \tag{8A}$$

recalling that

$$m = \frac{V_x}{a} = \frac{V_x}{\frac{kT}{q}}$$

From this it can be seen that voltage gain is a function of the input level supplied to the upper four transistors:

$$\frac{\Delta V_O}{V_{in}} = A_V = \frac{2R_L}{R_E}[f(m)] \tag{9A}$$

and

$$V_O = \frac{2R_LV_y}{R_E}[f(m)] \tag{10A}$$

A curve of f(m) versus input level supplied to the upper quad differential amplifier is shown in Figure 16 of the text.

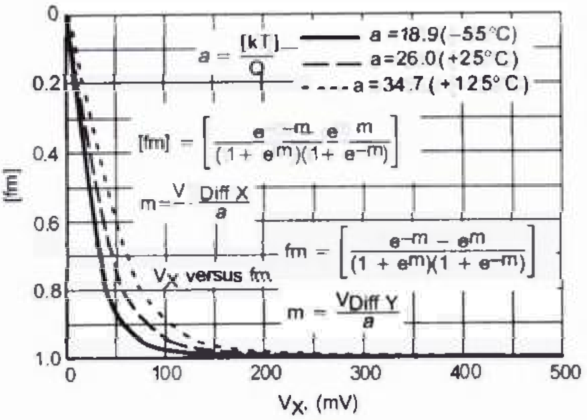

Figure 16. V_X versus [fm]

The MC1496 is therefore a linear multiplier over the range of V_X for which [f(m)] is a linear function of V_X. This range of x can be obtained by inspection of Figure 16 and is approximately zero to 50 millivolts.

Examining the case of a small signal V_X input level mathematically yields:

Assume

$$V_X \ll a \tag{11A}$$

Then:

$$e^m \leq 0.1 \tag{12A}$$

$$e^m \approx 1 + m \tag{13A}$$

$$e^{-m} \approx 1 - m$$

$$[f(m)] \approx \left[\frac{(1-m)-(1+m)}{(2+m)(2-m)}\right] = \left(\frac{-2m}{4-m^2}\right) \tag{14A}$$

$$\left(\frac{-2m}{4-m^2}\right) \approx \frac{-2m}{4} = \frac{-m}{2} \tag{15A}$$

Therefore

$$A_V = \frac{V_O}{V_y} = \frac{2R_L}{R_E}\left(\frac{(-m)}{2}\right) = \frac{-R_L m}{R_E} \tag{16A}$$

$$V_O = \frac{-R_L V_y m}{R_E} = \frac{-R_L V_y V_x}{R_E a} \tag{17A}$$

Equation (17A) shows that the MC1496 is a linear multiplier when $V_X \leq 2.6$ mV. However, as was observed by inspection of Figure 16 earlier, the device is capable of approximate linear multiplier operation when $V_X \leq 50$ mV.

For the case of a large signal V_X input level:

$$V_X \gg a \tag{18A}$$

$$e^m \gg 1 \tag{19A}$$

$$e^{-m} \ll 1$$

$$A_V = \frac{2R_L}{R_E}\left[\frac{-e^m}{e^m}\right] = \frac{-2R_L}{R_E} \tag{20A}$$

$$V_O = \frac{-2R_L V_y}{R_E} \tag{21A}$$

Equation (20A) indicates that in this mode the output level is independent of the level of V_X. This characteristic is useful in many communications applications of the MC1496.

Mathematical analysis for ac input signals is given below for two modes of operation which cover most applications of the MC1496. These modes are (1) V_X and V_y both low level sine waves, and (2) low level sine wave for V_y and a large signal input for V_X (either a high level sine wave or a square wave input) giving rise to a symmetrical switching operation of the upper differential amplifier quad, Q1, Q2, Q3, and Q4.

For sine wave input signals,

$$V_X = E_X \cos\omega_X t \tag{22A}$$

$$V_y = E_y \cos\omega_y t \tag{23A}$$

where E_X and E_y are the peak values of the x and y input voltages, respectively. Therefore,

$$V_O = KE_XE_y(\cos\omega_X t)(\cos\omega_y t) \tag{24A}$$

Performing this multiplication yields:

$$V_O = \frac{KE_XE_y}{2}\cos(\omega_X + \omega_y)t + \cos(\omega_X - \omega_y)t \tag{25A}$$

The second mode of operation can be analyzed by assuming square wave switching function in the upper differential amplifiers and applying Fourier analysis.

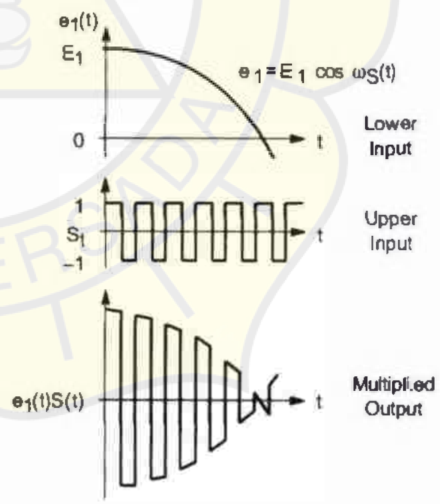

Figure 17. Input and Output Waveforms for a High Level Upper Input and Low Level Input Signals

The Fourier series form for the symmetrical square wave signal shown in Figure 17 is:

$$s(t) = 2\sum_{n=1}^{\infty} A_n \cos n\omega_x t \quad (26A)$$

where the Fourier coefficients are

$$A_n = \left[\frac{\sin\frac{\pi n}{2}}{\frac{\pi n}{2}}\right] \quad (27A)$$

The output voltage is therefore:

$$V_O = KE_y\sum_{n=1}^{\infty} A_n[\cos(n\omega_x + \omega_y)t + \cos(n\omega_x - \omega_y)t] \quad (28A)$$

Note that Equation (25A) predicts that for low level input signals, the output signal consists of the sum and difference frequencies ($\omega_x \pm \omega_y$) only, while Equation (28A) predicts that operation with a high level input for V_x input will yield outputs at frequencies $\omega_x \pm \omega_y$, $3\omega_x \pm \omega_y$, $5\omega_x \pm \omega_y$, etc.

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Email: r14525@onsemi.com

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LAMPIRAN 2

DATA SHEET

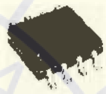
UA741 *General Purpose Single Operational Amplifier*

UA741

GENERAL PURPOSE SINGLE OPERATIONAL AMPLIFIER

- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGHGAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION
- REQUIRED
- SAME PIN CONFIGURATION AS THE UA709

N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The UA741 is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intented for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

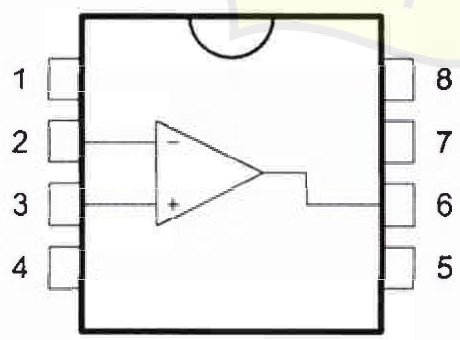
The high gain and wide range of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/octave) insures stability in closed loop circuits.

ORDER CODE

Part Number	Temperature Range	Package	
		N	D
UA741C	0°C, +70°C	•	•
UA741I	-40°C, +105°C	•	•
UA741M	-55°C, +125°C	•	•
Example : UA741CN			

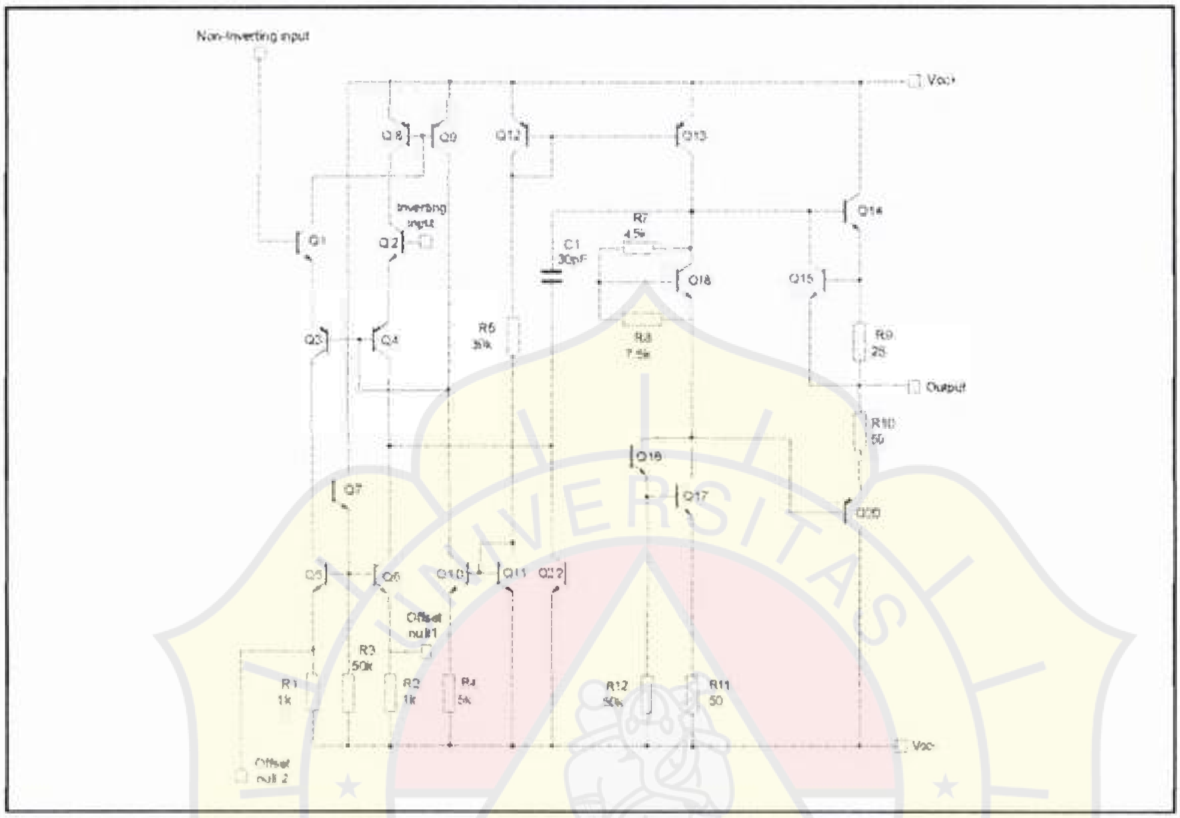
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UA741M	UA741I	UA741C	Unit
V_{CC}	Supply voltage		±22		V
V_{id}	Differential Input Voltage		±30		V
V_i	Input Voltage		±15		V
P_{tot}	Power Dissipation [1]		500		mW
	Output Short-circuit Duration		Infinite		
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range		-65 to +150		°C

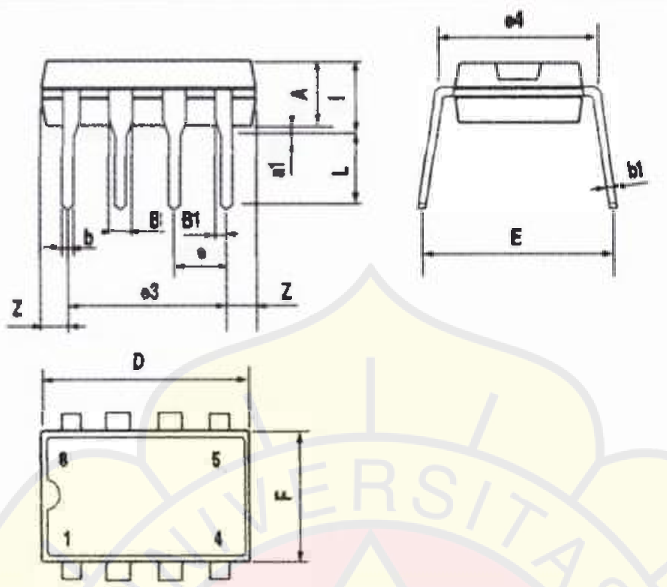
1. Power dissipation must be considered to ensure maximum junction temperature (Tj) is not exceeded.

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_{amb} = +25°C$ (unless otherwise specified)

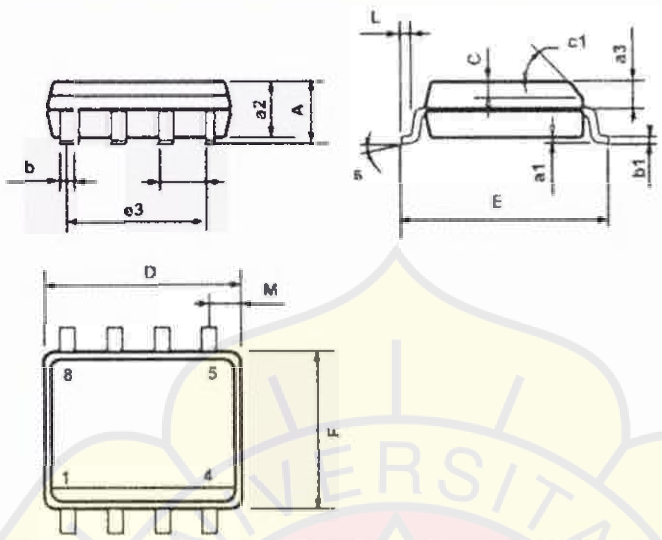
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_s \le 10k\Omega$) $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$		1	5 6	mV
I_{io}	Input Offset Current $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$		2	30 70	nA
I_{ib}	Input Bias Current $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$		10	100 200	nA
A_{vd}	Large Signal Voltage Gain ($V_o = \pm 10V$, $R_L = 2k\Omega$) $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_s \le 10k\Omega$) $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$	77 77	90		dB
I_{CC}	Supply Current, no load $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$		1.7	2.8 3.3	mA
V_{icm}	Input Common Mode Voltage Range $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$	±12 ±12			V
CMR	Common Mode Rejection Ratio ($R_S \le 10k\Omega$) $T_{amb} = +25°C$ $T_{min} \le T_{amb} \le T_{max}$	70 70	90		dB
I_{OS}	Output short Circuit Current	10	25	40	mA
$\pm V_{opp}$	Output Voltage Swing $T_{amb} = +25°C$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min} \le T_{amb} \le T_{max}$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	12 10 12 10	14 13		V
SR	Slew Rate $V_i = \pm 10V$, $R_L = 2k\Omega$, $C_L = 100pF$, unity Gain	0.25	0.5		V/μs
t_r	Rise Time $V_i = \pm 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, unity Gain		0.3		μs
K_{ov}	Overshoot $V_i = 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, unity Gain		5		%
R_i	Input Resistance	0.3	2		MΩ
GBP	Gain Bandwith Product $V_i = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$, f = 100kHz	0.7	1		MHz
THD	Total Harmonic Distortion f = 1kHz, $A_v = 20dB$, $R_L = 2k\Omega$, $V_o = 2V_{pp}$, $C_L = 100pF$, $T_{amb} = +25°C$		0.06		%
e_n	Equivalent Input Noise Voltage f = 1kHz, $R_s = 100\Omega$		23		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		50		Degrees

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

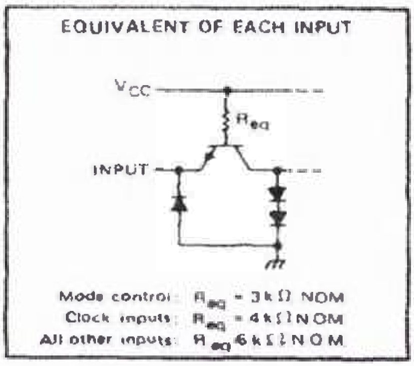
LAMPIRAN 3

DATA SHEET

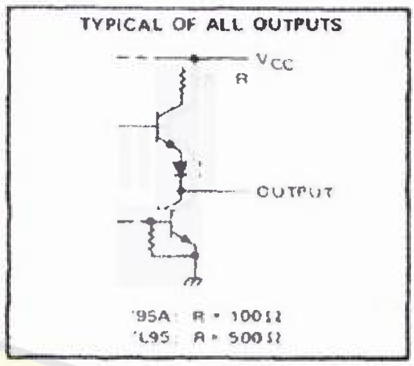
4-Bit Paralel – Access Shift Register

schematics of inputs and outputs

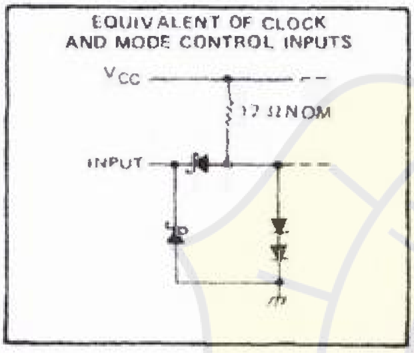
'95A



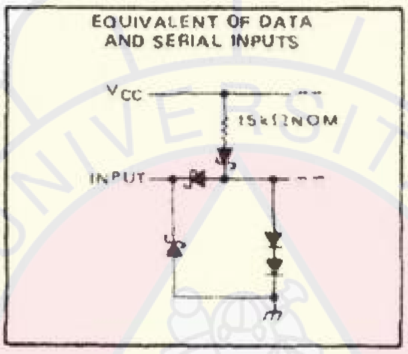
'95A



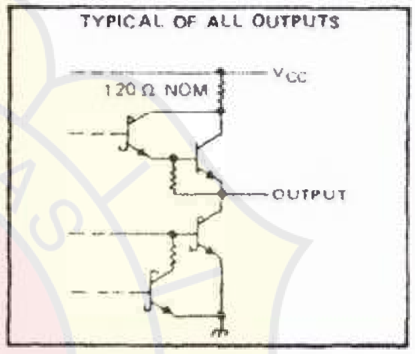
'LS95B



'LS95B



'LS95B



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	–55 to 125		0 to 70		°C
Storge temperature range	– 65 to 150		– 65 to 150		°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies between the clock-2 input and the mode control input of the '95A.

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