BAB V

KESIMPULAN

5.1 Kesimpulan

Dari pembahasan, pembuatan, pengujian serta hasil pengukuran yang telah dilakukan, dapat diambil kesimpulan sebagai berikut:

1. Rangkaian antarmuka jaringan telepon yang dibuat dapat berfungsi dengan baik,dimana sensor dapat mendeteksi ringging current. Demikian juga pada rangkaian lainya, sehingga dekoder DTMF dapat berfunsi dengan baik.
2. Pada rangkaian VMS maksimum waktu perekaman yang diperoleh dengan kapasitas memory 1 Mbit kurang lebih 45 detik.
3. Di dalam perancangan ini terjadi beberapa penyimpangan dari perhitungan yang didapat, karena nilai komponen hasil perhitungan tidak ada sehingga digunakan nilai komponen yang mendekati.

Dalam perancangan mesin penjawab telepon ini selain mengunakan perhitungan juga digunakan sistem coba-coba untuk mendapatkan hasil yang maksimal.

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Jakarta, Agustus 1997

(Suhairi)

National Semiconductor

Voltage Comparators

LM311 voltage comparator

general description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

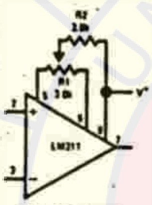
features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

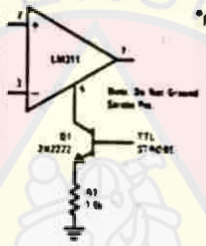
Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C. See the "application hints" of the LM311 for application help.

auxiliary circuits*

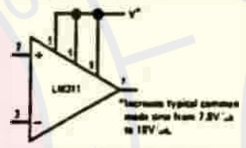
*Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing

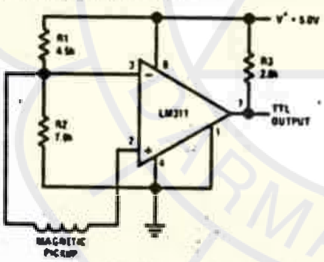


Strobing

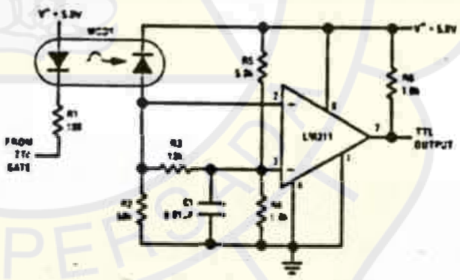


Increasing Input Stage Current*

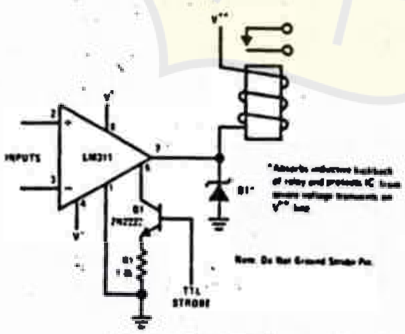
typical applications*



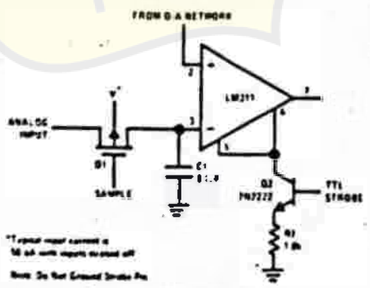
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe



Strobing off Both Input* and Output Stages

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Voltage at Strobe Pin	V^+-5 V

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	T_A = 25°C		6.0	50	nA
Input Bias Current	T_A = 25°C		100	250	nA
Voltage Gain	T_A = 25°C	40	200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, I_{OUT} = 50 mA T_A = 25°C		0.75	1.5	V
Strobe ON Current	T_A = 25°C		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, V_{OUT} = 35V T_A = 25°C, I_{STROBE} = 3 mA		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8, −14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5$ V, V^- = 0 $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	T_A = 25°C		5.1	7.5	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for V_S = ±15V and the Ground pin at ground, and 0°C < T_A < +70°C, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

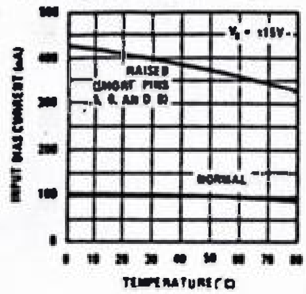
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

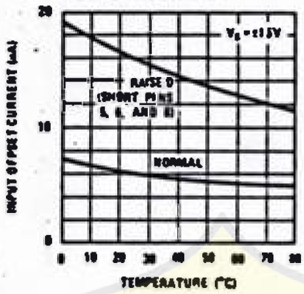
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

typical performance characteristics

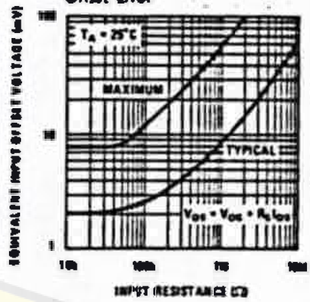
Input Bias Current



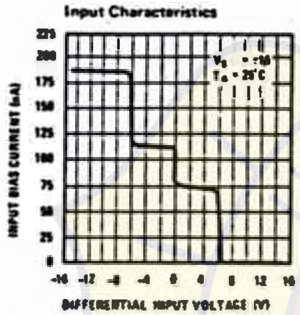
Input Offset Current



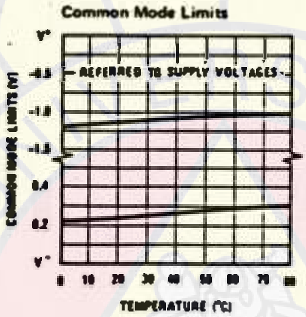
Offset Error



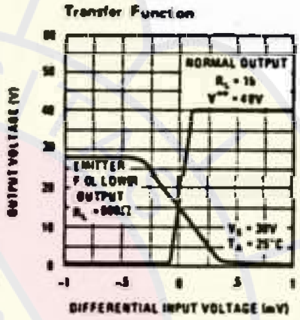
Input Characteristics



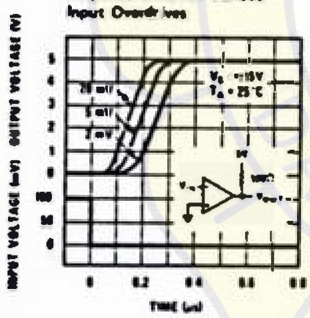
Common Mode Limits



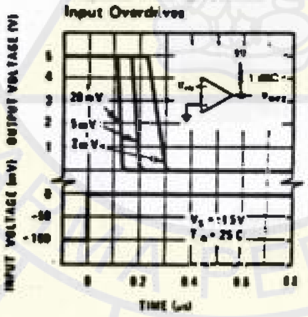
Transfer Function



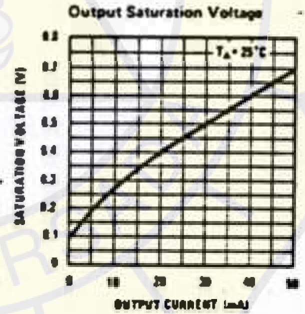
Response Time for Various Input Overdrives



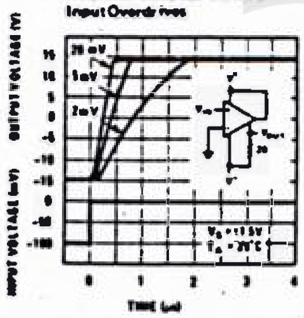
Response Time for Various Input Overdrives



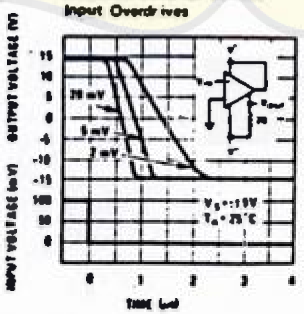
Output Saturation Voltage



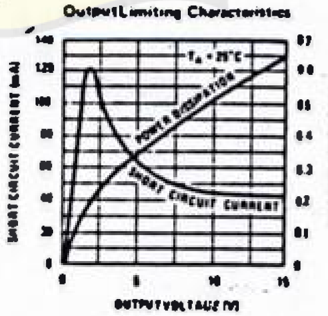
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

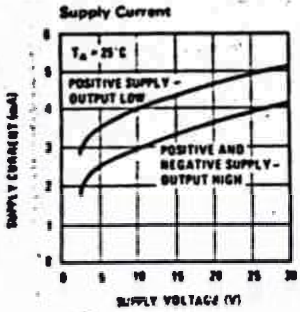


Output Limiting Characteristics

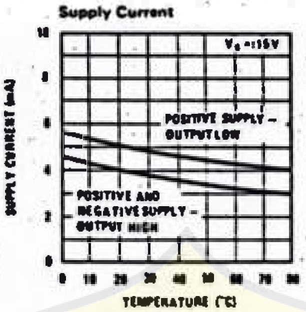


typical performance characteristics (con't)

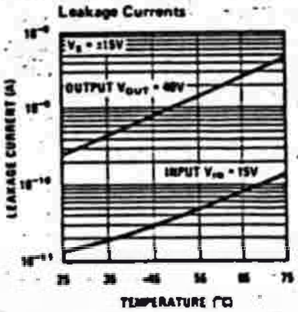
Supply Current



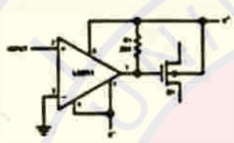
Supply Current



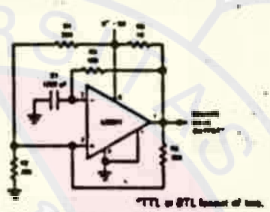
Leakage Currents



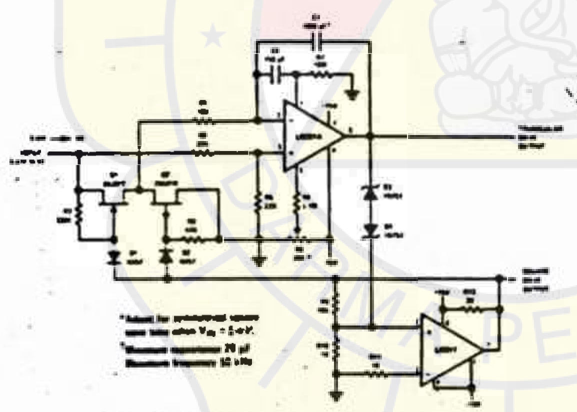
typical applications



Zero Crossing Detector Driving MOS Switch

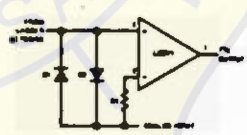


100 kHz Free Running Multivibrator

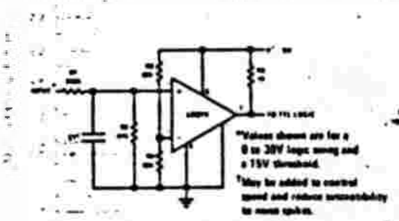


10 Hz to 10 kHz Voltage Controlled Oscillator

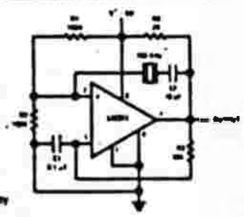
Driving Ground-Referred Load



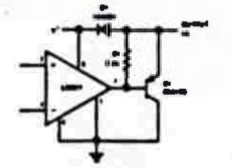
Using Clamp Diodes to Improve Response



TTL Interface with High Level Logic

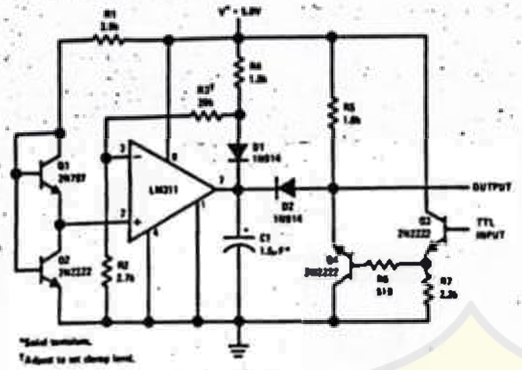


Crystal Oscillator

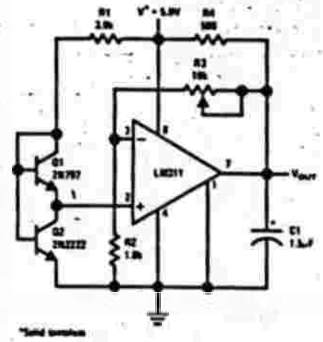


Comparator and Solenoid Driver

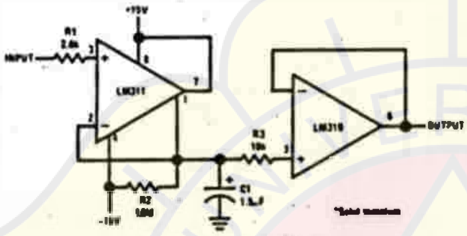
typical applications (con't)



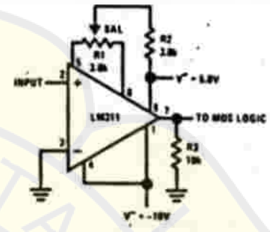
Precision Squarer



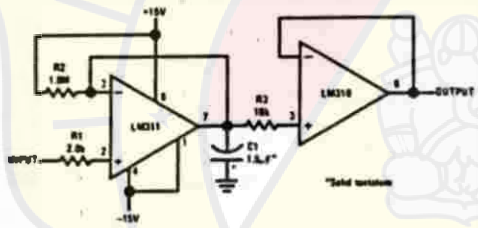
Low Voltage Adjustable Reference Supply



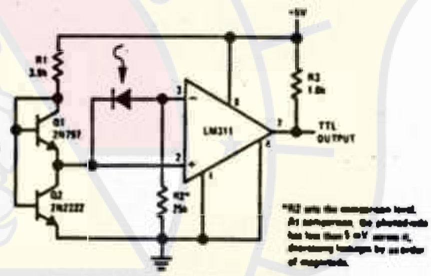
Positive Peak Detector



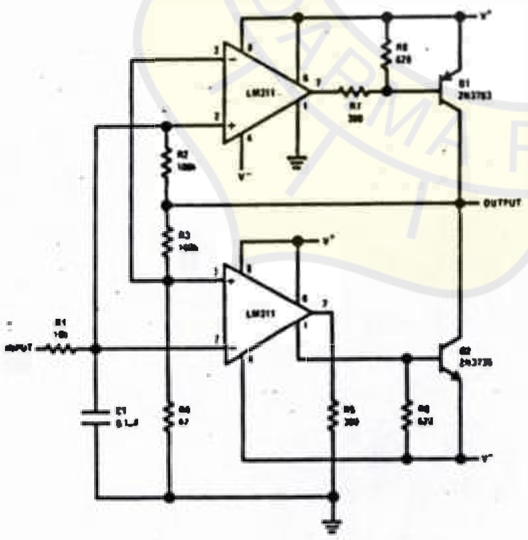
Zero Crossing Detector driving MOS logic



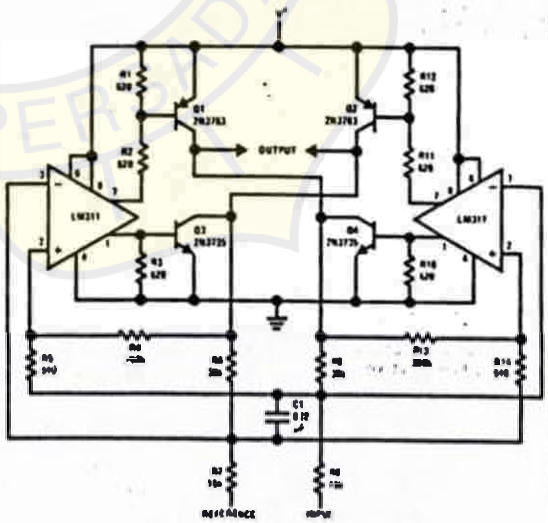
Negative Peak Detector



Precision Photodiode Comparator

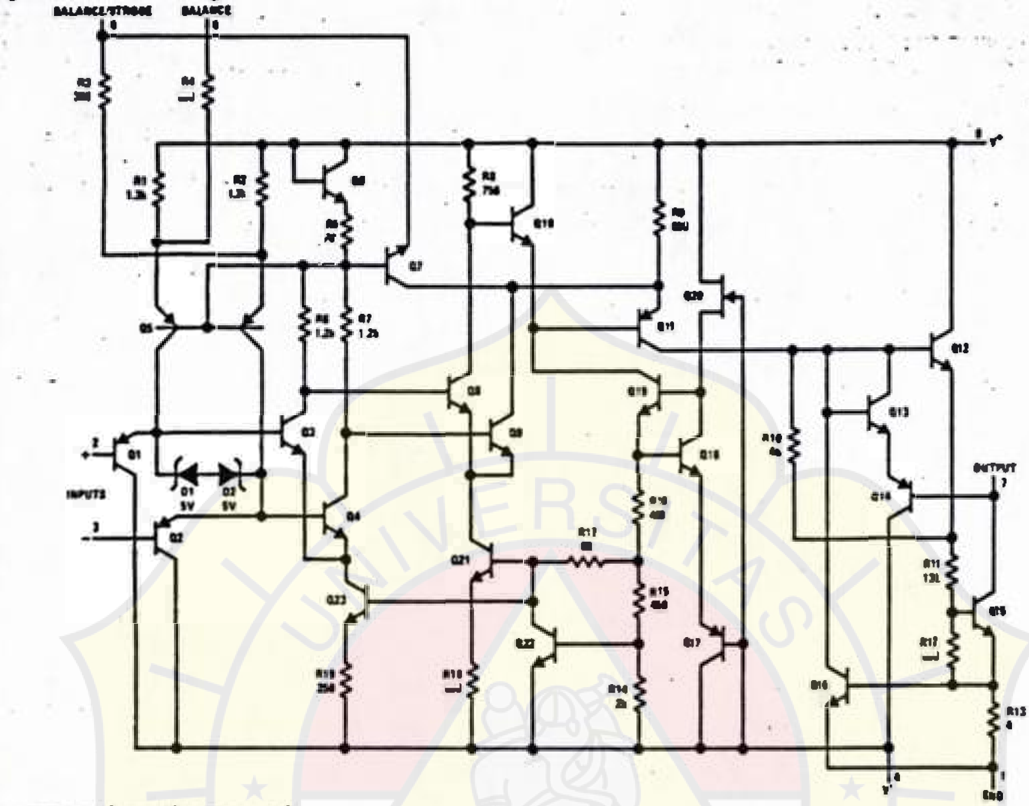


Switching Power Amplifier



Switching Power Amplifier

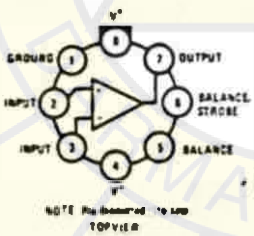
schematic diagram



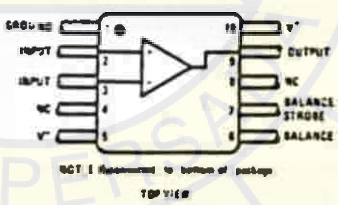
connection diagrams *

Metal Can Package

Order Number LM311H
See NS Package H08C



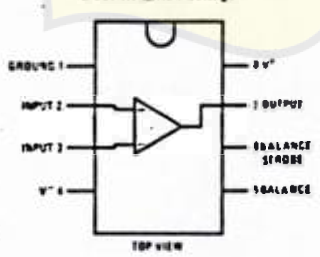
Flat Package



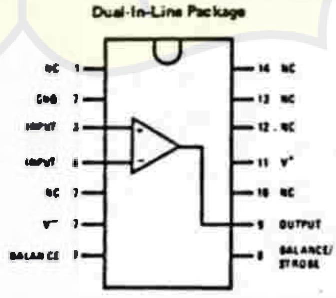
Order Number LM311F
See NS Package F10A

Dual-In-Line Package

Order Number LM311N
See NS Package N08B
Order Number LM311J-8
See NS Package J08A



Dual-In-Line Package



Order Number LM311D
See NS Package D14E
Order Number LM311N-14
See NS Package N14A
Order Number LM311J
See NS Package J14A

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

application hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

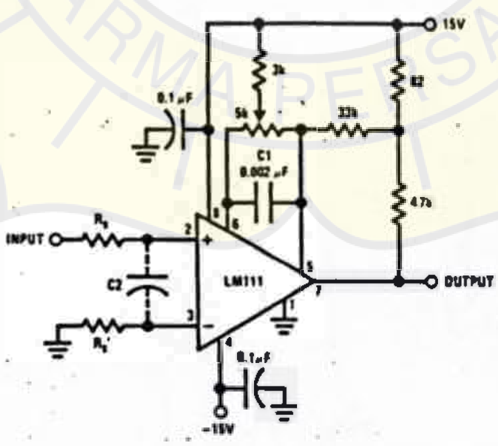
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.

2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

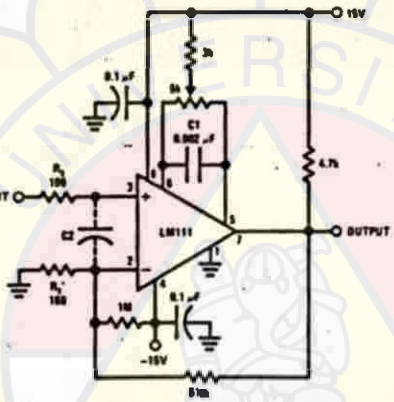
FIGURE 1. Improved Positive Feedback

application hints (con't)

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.

7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback

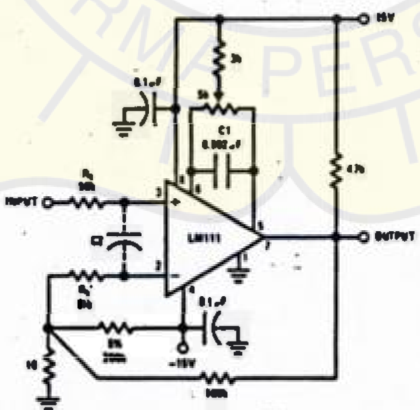


FIGURE 3. Positive Feedback With High Source Resistance

National Semiconductor

Industrial/Automotive/Functional Blocks/ Telecommunications

LM555/LM555C timer

general description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

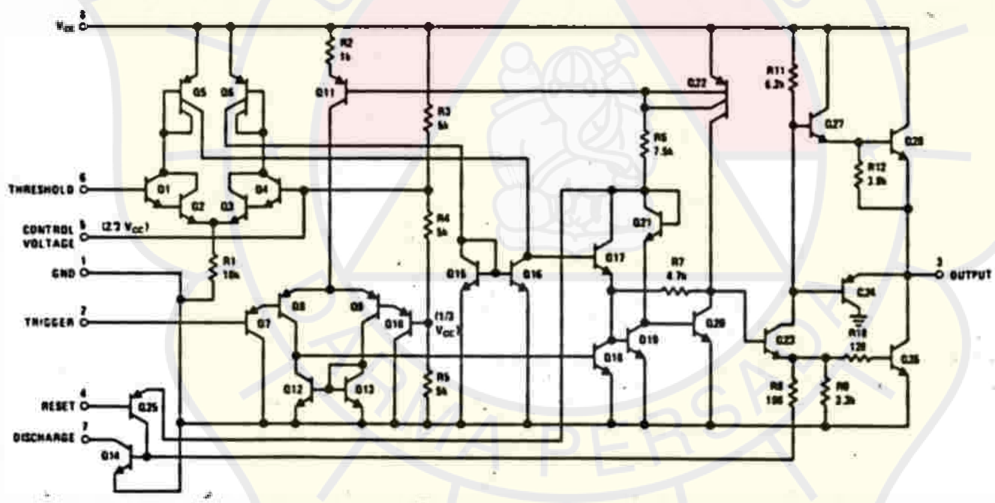
features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

applications

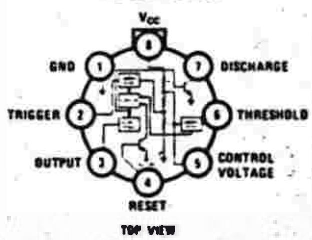
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

schematic diagram



connection diagrams

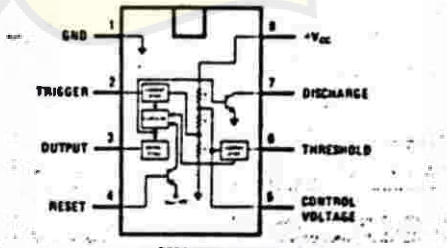
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM555CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

absolute maximum ratings

Supply Voltage	+18 V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5	2		1		%
Drift with Temperature	R_A, R_B = 1k to 100k, C = 0.1µF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5	3.0		1.5		%
Drift with Supply			0.05	0.2		0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5	5		2.25	7	%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15	0.2		0.30	0.5	%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	µA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

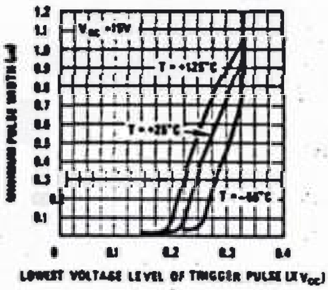
Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

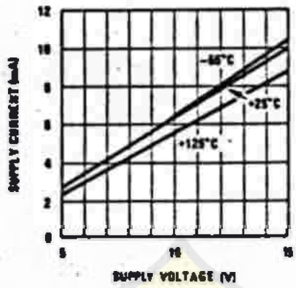
Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

typical performance characteristics

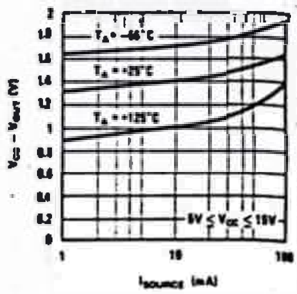
Minimum Pulse Width Required for Triggering



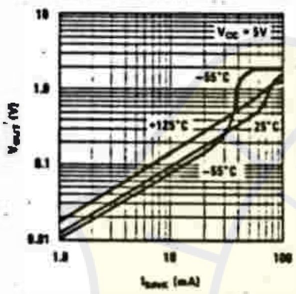
Supply Current vs Supply Voltage



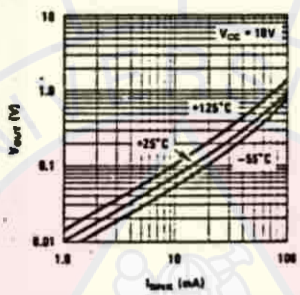
High Output Voltage vs Output Source Current



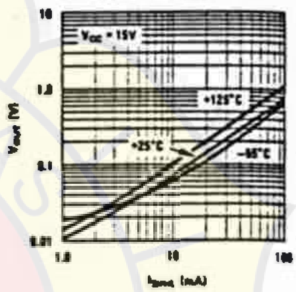
Low Output Voltage vs Output Sink Current



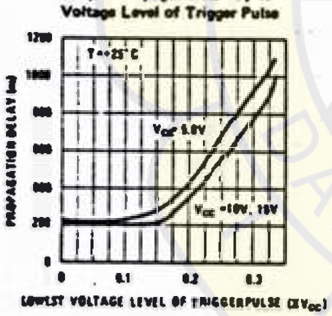
Low Output Voltage vs Output Sink Current



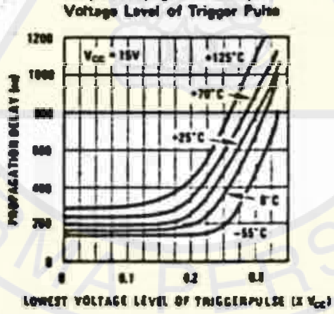
Low Output Voltage vs Output Sink Current



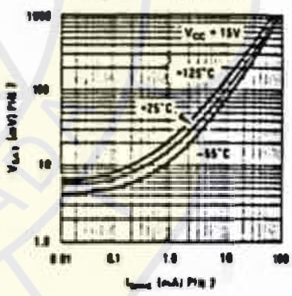
Output Propagation Delay vs Voltage Level of Trigger Pulse



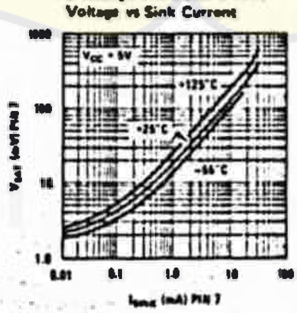
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



applications information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than $1/3 V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

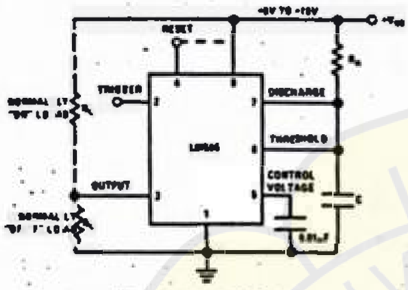


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals $2/3\ V_{CC}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

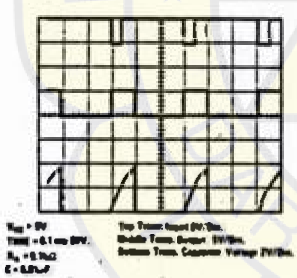


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

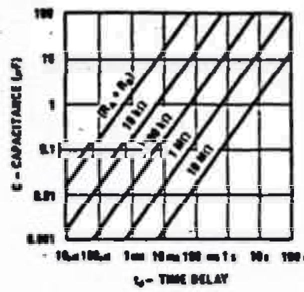


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

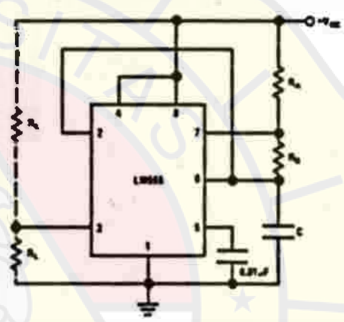


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between $1/3\ V_{CC}$ and $2/3\ V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

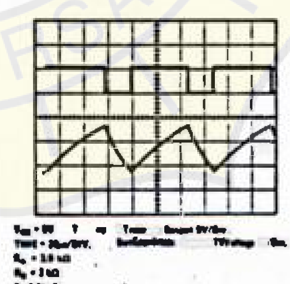


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693(R_A + R_B)C$$

And the discharge time (output low) by:

$$t_2 = 0.693(R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693(R_A + 2R_B)\ C$$

applications information (con't)

The frequency of oscillation is

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is

$$D = \frac{R_B}{R_A + 2R_B}$$

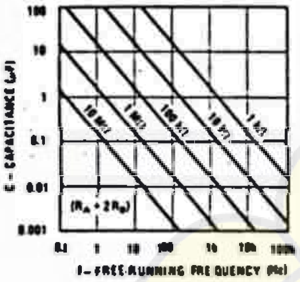


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

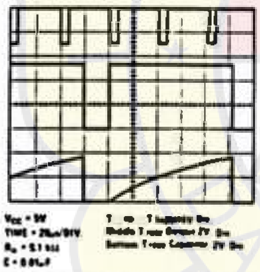


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

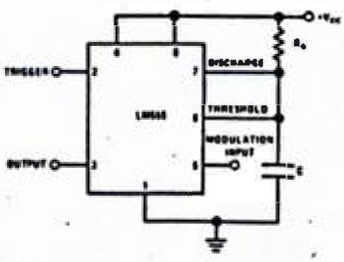


FIGURE 8. Pulse Width Modulator

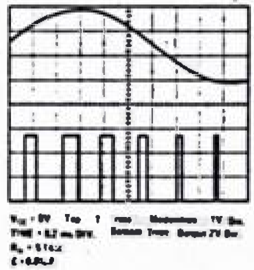


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

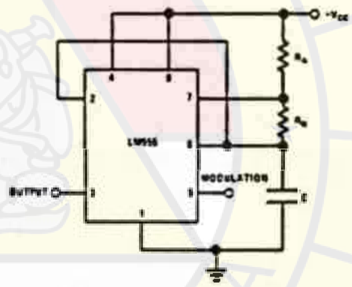


FIGURE 10. Pulse Position Modulator

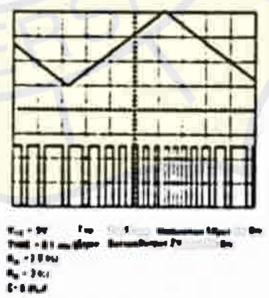


FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

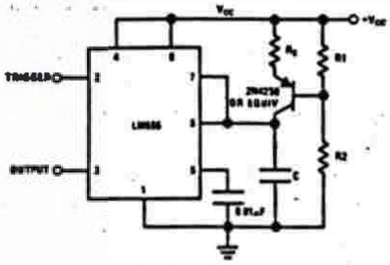


FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$$V_{BE} \approx 0.6V$$

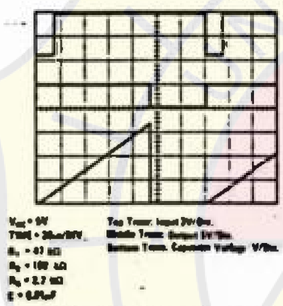


FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$[(R_A\ R_B)/(R_A + R_B)]\ C\,Ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

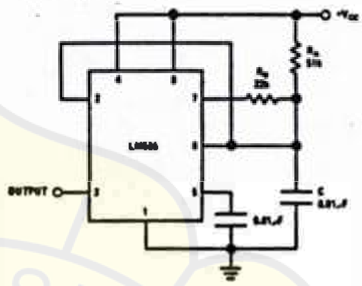


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than $1/2\ R_A$ because the junction of R_A and R_B cannot bring pin 2 down to $1/3\ V_{CC}$ and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

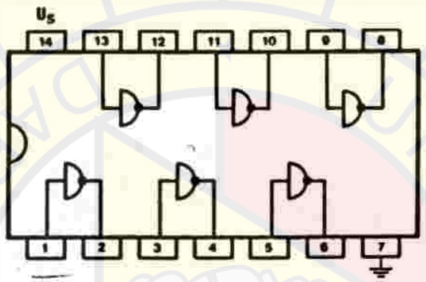
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

7404 /1

Inverters with totem-pole outputs

Function table see section 1



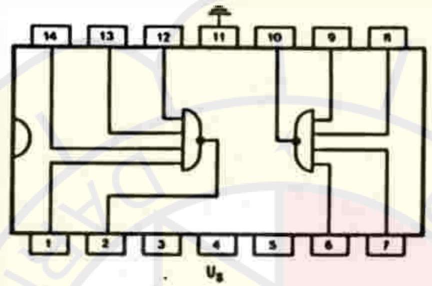
7404 /1 T_U = 0...70°C / -55...75°C	Type T_U = -25...85°C / -40...85°C	Type T_U = -55...125°C	Manufact.	B Bauf.	P_{typ} / P_{max} mW	E→Q		E→Q		Bem. - Note
FJH 241			Phi,Sig,Val	Sa	63	8	12	≤15	≤22	
FLH 211	FLH 215		Sie,Tun	Sa	63	8	12	≤15	≤22	
HD 7404			Hit	Sa	60	8	12	≤15	≤22	
M 53204			Mit	Sa	60	8	12	≤15	≤22	
MB 416			Fuj	Sa	60	8	12	≤15	≤22	
MIC 7404 J		MIC 5404 J	ITT	Sb	63	8	10	≤15	≤22	
MIC 7404 N		MIC 5404 N	ITT	Sa	63	8	10	≤15	≤22	
N 7404 A		S 5404 A	Mul,Phi,Sig	Sa	63	8	12	≤15	≤22	
N 7404 F		S 5404 F	Mul,Phi,Sig	Sb	63	8	12	≤15	≤22	
SN 7404 J		SN 5404 J	Tin	Sc	60	8	12	≤15	≤22	
SN 7404 N	SN 8404 N	SN 5404 N	Tin	Sa	60	8	12	≤15	≤22	
T 7404 B1			SGS	Sa	63	8	12	≤15	≤22	
T 7404 D1		T 5404 D2	SGS	Sa	63	8	12	≤15	≤22	
TD 3404			Tos	Sb Sa	60	8	9	≤15	≤22	
TL 7404 N	TL 8404 N		AEG	Sa	63	8	9	≤15	≤22	
U6A 7404 59X		U7A 5404 51X	Fch	Sa						
U7A 7404 59X		U7A 5404 51X	Fch	Sa						
μPB 226			Nip	Sa	60	8	12	≤15	≤22	

7404 /1 T_U = 0...70°C / -55...75°C	Type T_U = -25...85°C / -40...85°C	Type T_U = -55...125°C	Manufact.	B Bauf.	P_{typ} / P_{max} mW	E→Q		E→Q		Bem. - Note
H										
N 74H04 A		S 54H04 A	Mul,Phi,Sig	Sa	140	6.5	9	≤10	≤12	
N 74H04 F		S 54H04 F	Mul,Phi,Sig	Sb	140	6.5	9	≤10	≤12	
SN 74H04 J		SN 54H04 J	Tin		135	6.5	9	≤10	≤10	
SN 74H04 N		SN 54H04 N	Tin	Sa	135	6.5	9	≤10	≤10	
L										
SN 74L04 J		SN 54L04 J	Tin	Sc	6	31	35	≤60	≤60	
SN 74L04 N	SN 84L04 N	SN 54L04 N	Tin	Sa	6	31	35	≤60	≤60	
LS										
HD 74LS04			Hit	Sa	12	10	9	≤15	≤15	
SN 74LS04 J		SN 54LS04 J	Tin	Sc	12	10	9	≤15	≤15	
SN 74LS04 N		SN 54LS04 N	Tin	Sa	12	10	9	≤15	≤15	
SN 74LS04 N-S4			Tin	Sa	12	10	9	≤15	≤15	E: 15V
S										
HD 74S04			Hit	Sa	112	3	3	≤5	≤4.5	
MSS 804			Mit	Sa	112	3	3	≤5	≤4.5	
N 74S04 A		S 54S04 A	Mul,Phi,Sig	Sa	112	3	3	≤5	≤4.5	
N 74S04 F		S 54S04 F	Mul,Phi,Sig	Sb	112	3	3	≤5	≤4.5	
N 74S04 W		S 54S04 W	Mul,Phi,Sig	15b	112	3	3	≤5	≤4.5	
SN 74S04 J		SN 54S04 J	Tin	Sc	112	3	3	≤5	≤4.5	
SN 74S04 N		SN 54S04 N	Tin	Sa	112	3	3	≤5	≤4.5	
SN 74S04 W		SN 54S04 W	Tin	15b	112	3	3	≤5	≤4.5	
μPB 2904			Nip	Sa	112	3	3	≤5	≤4.5	

7420 /2

NAND gate with totem pole outputs

Function table see section 1

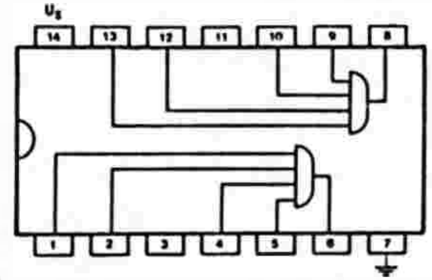


7420 /2 T_U = 0...70°C	Type T_U = −25...85°C	Type T_U = −55...125°C	Manufact.	B	P_{typ} mW	tp E → Q typ		max	tp E → Q typ		max	f_T MHz	U V
		DM 5420 W	Nsc	15b	20						≤29		
MC 7420 F		MC 5420 F	Mot	15c	20		13						
		MCB 5420 F	Mot	15d	20		10						
		S 5420 W	Mul,Phi,Sig	15b	20	5		12	≤15		≤22		
SN 7420 W		SN 5420 W	Tex	15b	20	5		12	≤15		≤22		
US 7420 J		US 5420 J	Spr	15b					50		≤15		
ZN 7420 F		ZN 5420 F	Fer	15d	10						≤29		
H													
		S 54H20 W	Mul,Phi,Sig	15b	45	7		6	≤10		≤10		
SN 74H20 W		SN 54H20 W	Tex	15b	45	7		6	≤10		≤10		
US 74H20 J		US 54H20 J	Spr	15b					≤10		≤10		
L													
DM 74L20 F		DM 54L20 F	Nsc	15d	2					≤110			
SN 74L20 T		SN 54L20 T	Tex	15c	2	31		35	≤60		≤60		

7421 /1

AND gate with totem pole outputs

Function table see section 1

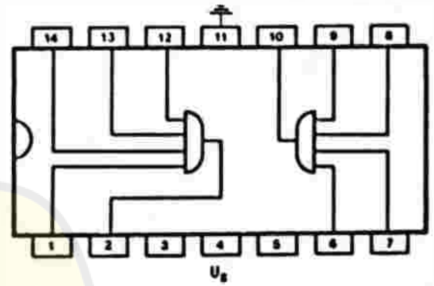


7421 /1 T_U = 0...70°C	Type T_U = −25...85°C	Type T_U = −55...125°C	Manufact.	B	P_{typ} mW	tp E → Q typ		max	tp E → Q typ		max	f_T MHz	U V
MIC 7421 J	SMIC 8421 J	MIC 5421 J	ITT	5b	40	12		17,5	≤18		≤27		
MIC 7421 N			ITT	5a	40	12		17,5	≤18		≤27		
N 7421 A		S 5421 A	Mul,Phi,Sig	5a	20	8		17	≤18		≤22		
N 7421 F		S 5421 F	Mul,Phi,Sig	5b	20	8		17	≤15		≤22		
TD 3421			Tos	5a	42,5	12		18	≤18		≤27		
H													
DM 74H21 J		DM 54H21 J	Nsc	5b	≤100					≤12			
DM 74H21 N		DM 54H21 N	Nsc	5a	≤100					≤12			
MIC 74H21 J			ITT	5b			8						
N 74H21 A		S 54H21 A	Mul,Phi,Sig	5a	80	8,8		7,8	≤12		≤12		
N 74H21 F		S 54H21 F	Mul,Phi,Sig	5b	80	8,8		7,8	≤12		≤12		
MC 74H21 N			Mot	5a						≤15			
SFC 421 HE		SFC 421 HEM	Mot,Ses	5b						≤12			
SN 74H21 J		SN 54H21 J	Tex	5c	80	8,8		7,8	≤12		≤12		
SN 74H21 N		SN 54H21 N	Tex	5a	80	8,8		7,8	≤12		≤12		
T 74H21 B1			SGS	5a	80		8						
T 74H21 D1		T 54H21 D2	SGS	5b	80		8						
US 74H21 A		US 54H21 A	Spr	5b					≤10		≤18		

7421 /1	Type		Manufact.	Gehäuse	P_{typ}	E → O			E → O			f_T	U
T_U = 0...70 °C / 10...75 °C	T_U = −25...85 °C / −40...85 °C	T_U = −55...125 °C		3	mW							MHz	V
LS													
N 74LS21 A			Mul,Phi,Sig	6a	22		12						
N 74LS21 F			Mul,Phi,Sig	6b	22		12						
SN 74LS21 J		SN 54LS21 J	Tix	6c	8,8	12		12	≤20		≤15		
SN 74LS21 N		SN 54LS21 N	Tix	6a	8,8	12		12	≤20		≤15		
SN 74LS21 W		SN 54LS21 W	Tix	15b	8,8	12		12	≤20		≤15		
9LS21 DC 1)		9LS21 DM 1)	Fch	6b	≤22		10						
9LS21 FC 1)		9LS21 FM 1)	Fch	15d	≤22								
9LS21 PC 1)			Fch	6a	≤22		10						
74LS21 DC 1)		54LS21 DM 2)	Fch	6b	≤22		10						
74LS21 FC 1)		54LS21 FM 2)	Fch	15d	≤22		10						
		54LS21 J	Ray	6b	≤220		10						
74LS21 PC 1)			Fch	9b	≤22		10						
		54LS21 W	Ray	15d	≤220		10						
S													
TG 74S21 J		TG 54S21 J	Tro	6b	≤70				≤7,5				
1) FQ-5		2) FQ-2,5											

7421 /2

AND gate with totem pole outputs



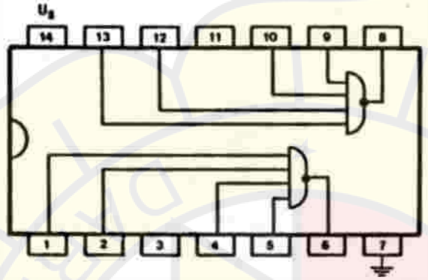
Function table see section 1

7421 /2	Type		Manufact.	Gehäuse	P_{typ}	E → O			E → O			f_T	U
T_U = 0...70 °C / 10...75 °C	T_U = −25...85 °C / −40...85 °C	T_U = −55...125 °C		3	mW							MHz	V
		S 5421 W	Mul,Phi,Sig	15b	20	8		12	≤15		≤22		
H													
		S 54H21 W	Mul,Phi,Sig	15b	80	8,8		7,6	≤12		≤12		
SN 74H21 W		SN 54H21 W	Tix	15b	80	8,8		7,6	≤12		≤12		
US 74H21 J		US 54H21 J	Spr	15b					≤10		≤10		
S													
TG 74S21 F		TG 54S21 F	Tro	15d	≤70					≤7,5			

7440 /1

NAND gate with totem-pole outputs (FQ = 30)

Function table see section 1



7440 /1 T_U = 0...70°C	Type T_U = −25...85°C / −40...85°C	T_U = −55...125°C	Manufact.	B	P_{typ} mW	E → Q		E → Q		f_T MHz	Note V
D 140 C	E 140 C		HFO	Se	50	10	14,5	≤15	≤22		
D 140 D			HFO	Se	50	10	14,5	≤15	≤22		
DM 7440 J		DM 5440 J	Nsc	Sb	≤114				≤75		
DM 7440 N		DM 5440 N	Nsc	Se	≤114				≤75		
FJH 141			Phi,Sig,Val	Se	52,5	5	13	≤15	≤22		
FLH 141	FLH 140		Sie,Tes	Se	52,5	9	13	≤15	≤22		
GFB 7440			RTC	Sb	52		13				
HD 7440			Hit	Se	52,5	8	13	≤15	≤22		
IDT 7440				Se	50	10	14,5	≤15	≤22		
ITT 7440 J			ITT	Sc	20				≤22		
M 53240			Mis	Se	52,5	8	13	≤15	≤22		
MB 404			Fuj	Se	52,5	8	13	≤15	≤22		
MC 7440 L		MC 5440 L	Mot	Sb	60		13				
MIC 7440 J	MIC 8440 J	MIC 5440 J	ITT	Sb	53	5	10	≤15	≤22		
MIC 7440 N			ITT	Se	53	3	10	≤15	≤22		
MH 7440	MH 8440		Tes	Se	50	10	14,5	≤15	≤22		
N 7440 A		S 5440 A	Mul,Phi,Sig	Se	52,5	8	13	≤15	≤22		
N 7440 F		S 5440 F	Mul,Phi,Sig	Sb	52,5	8	13	≤15	≤22		
NC 7440 N			Nuc	Se	40		13				
SFC 440 E	SFC 440 ET	SFC 440 EM	Nuc,Ses	Sb	≤130		13		≤22		

7440 /1 T_U = 0...70°C	Type T_U = −25...85°C / −40...85°C	T_U = −55...125°C	Manufact.	B	P_{typ} mW	E → Q		E → Q		f_T MHz	Note V
SN 7440 J		SN 5440 J	Tix	Sc	52,5	8	13	≤15	≤22		
SN 7440 N	SN 8440 N	SN 5440 N	Tix	Se	52,5	8	13	≤15	≤22		
	SBN 8440 N		Tix	Se	52,5	8	13	≤15	≤22		
SW 7440 J			Stw	Sg	564			≤13			
SW 7440 N			Stw	Se	564			≤13			
ST 100 D1			SGS	Se	86			≤10	≤15		
ST 100 D1		T 100 D2	SGS	Sb	86			≤10	≤15		
T 7440 B1			SGS	Se	52,5	8	13	≤15	≤22		
T 7440 D1		T 7440 D2	SGS	Sb	52,5	8	13	≤15	≤22		
TD 3440			Tos	Se	52,5	8	13	≤15	≤22		
TL 7440 N	TL 8440 N		AEG	Se	52,5	8	13	≤15	≤22		
UCA 7440 50X		UCA 5440 51X	Fch	Sb							
UJA 7440 50X		UJA 5440 51X	Fch	Se							
US 7440 A		US 5440 A	Spr	Sb		8	10				
μPB 206			Nip	Se	52,5	8	13	≤15	≤22		
1 LB 556			SU	Se	50	10	14,5	≤15	≤22		
H											
D 240 C			HFO	Se	75	5	7	≤12	≤12		
DM 74H40 J		DM 54H40 J	Nsc	Sb	≤200			≤12			
DM 74H40 N		DM 54H40 N	Nsc	Se	≤200			≤12			
GJB 74H40 P			RTC	Se	92			≤12			
MIC 74H40 J			ITT	Sb				≤10			
N 74H40 A		S 54H40 A	Mul,Phi,Sig	Se	88	6,5	6,5	≤12	≤12		
N 74H40 F		S 54H40 F	Mul,Phi,Sig	Sb	88	6,5	6,5	≤12	≤12		
NC 74H40 N			Nuc	Se				≤10			
SFC 440 HE		SFC 440 HEM	Nuc,Ses	Sb	40	5		≤10			
SN 74H40 J		SN 54H40 J	Tix	Sc	88	6,5	6,5	≤12	≤12		
SN 74H40 N		SN 54H40 N	Tix	Se	88	6,5	6,5	≤12	≤12		
T 74H40 B1			SGS	Se	80	8					
T 74H40 D1		T 54H40 D2	SGS	Sb	80	8					
US 74H40 A		US 54H40 A	Spr	Sb				≤10	≤75		
1 LB 316			SU	Se	75	5	7	≤12	≤12		
LS											
SN 74LS40 J		SN 54LS40 J	Tix	Sc	8,8	12	12	≤24	≤24		FO=60
SN 74LS40 N		SN 54LS40 N	Tix	Se	8,8	12	12	≤24	≤24		FO=60
SN 74LS40 W		SN 54LS40 W	Tix	Flb	8,8	12	12	≤24	≤24		FO=60
9LS40 DC [1]		9LS40 DM [1]	Fch	Sb	≤30	10					
9LS40 FC [1]		9LS40 DM [2]	Fch	1bd	≤30	10					
9LS40 PC [1]			Fch	Se	≤30	10					
74LS40 DC [1]		54LS40 DM [2]	Fch	Sb	≤30	10					
74LS40 FC [1]		54LS40 FM [2]	Fch	1bd	≤30	10					
		54LS40 J	Ray		≤30	7					FO=60
74LS40 PC [1]			Fch	Se	≤30	10					
		54LS40 W	Ray	1bd	≤30	7					FO=60
1) FO=15		2) FO=7,5									