BAB V

KESIMPULAN

1. Modulasi *Quadrature Phase shift keying* (QPSK) menghasilkan 4 fasa yang berbeda, terdiri dari 2 bit atau simbol sesuai dengan prinsip modulasi QPSK.
2. Sinyal termodulasi QPSK merupakan jumlah dari 2 sinyal kanal Q (cos dan – cos) dan 2 sinyal kanal I (sin dan – sin) yang membentuk 4 kombinasi. Hasil pengujian dari input data sinyal 00,01,10,11 menghasilkan pergeseran phasa 90^0,180^0,90^0,180^0.
3. Setelah melalui pengujian di laboratorium, modulator QPSK yang dirancang dan sudah bekerja sesuai dengan apa yang diharapkan di mana pada outputnya menghasilkan sinyal termodulasi QPSK yang akan di kirim ke demodulator.
4. QPSK adalah modulasi dengan amplitudo yang sama dengan phasa berubah-ubah, untuk mendapatkan amplitudo yang sama dengan cara mengatur potensiometer 50k Ohm pada rangkaian balanced modulator kanal I dan kanal Q.

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LAMPIRAN 1

DATA SHEET

MC 1496 BALANCE MODULATOR

AN531/D

MC1496 Balanced Modulator

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Applications Engineering

ON Semiconductor
http://onsemi.com

APPLICATION NOTE

INTRODUCTION

The ON Semiconductor MC1496 monolithic balanced modulator makes an excellent building block for high frequency communications equipment.

The device functions as a broadband, double–sideband suppressed carrier balanced modulator without a requirement for transformers or tuned circuits. In addition to its basic application as a balanced modulator/demodulator, the device offers excellent performance as an SSB product detector, AM modulator/detector, FM detector, mixer, frequency doubler, phase detector, and more.

The article consists of a general description of the MC1496, its gain equations, biasing information, and circuits illustrating typical applications. It is followed by an appendix containing a detailed mathematical ac and dc analysis of the device.

Many readers may find that one of the circuits described in the article will fill the needs of their application. However, it is impossible to show typical circuits for every possible requirement, and the detailed analysis given in the appendix will assist the designer in developing an optimum circuit for any application within the basic capabilities of the MC1496.

MC1496 General Description

Figure 1 shows a schematic diagram of the MC1496. For purposes of the analysis, the following conventional assumptions have been made for simplification: (1) Devices of similar geometry within a monolithic chip are assumed identical and matched where necessary, and (2) transistor base currents are ignored with respect to the magnitude of collector currents; therefore, collector and emitter currents are assumed equal.

Referring to Figures 1 and 2, the MC1496 consists of differential amplifier Q5 Q6 driving a dual differential amplifier composed of transistors Q1, Q2, Q3 and Q4. Transistors Q7 and Q8 and associated bias circuitry form constant current sources for the lower differential amplifier Q5 Q6.

The analysis of operation of the MC1496 is based on the ability of the device to deliver an output which is proportional to the product of the input voltages V_X and V_Y. This holds true when the magnitudes of V_X and V_Y are maintained within the limits of linear operation of the three differential amplifiers in the device. Expressed mathematically, the output voltage (actually output current, which is converted to an output voltage by an external load resistance), V_O is given by

$$V_O = KV_XV_Y \quad (1)$$

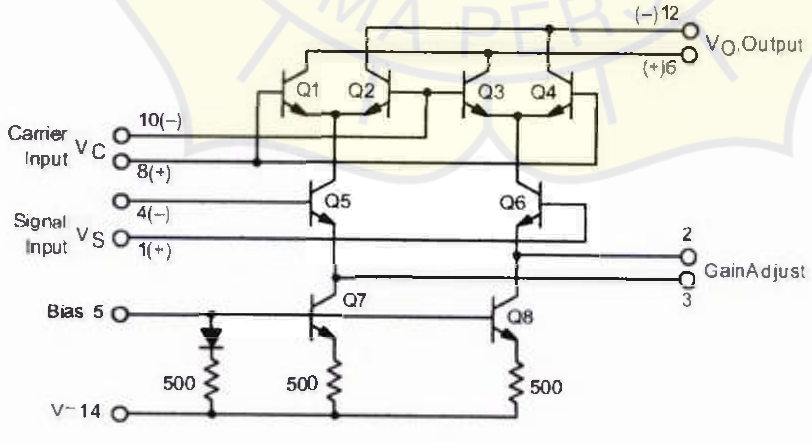

Figure 1. MC1496 Schematic

transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\ \text{Vdc} \geq [(V_6, V_{12}) - (V_8, V_{10})] \geq 2\ \text{Vdc}$$
$$30\ \text{Vdc} \geq [(V_8, V_{10}) - (V_1, V_4)] \geq 2.7\ \text{Vdc}$$
$$30\ \text{Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7\ \text{Vdc}$$

The foregoing conditions are based on the following assumptions:

$$V_6 = V_{12},\ V_8 = V_{10},\ V_1 = V_4$$

The other consideration in bias design is total device dissipation, which must not exceed 680 mW and 575 mW at $T_A = 25°C$, respectively, for the metal and ceramic dual in-line packages.

From the assumptions made above total device dissipation may be computed as follows:

$$P_D = 2I_5(V_6 - V_{14}) + I_5(V_5 - V_{14}) \quad (19)$$

For examples of various bias circuit designs, refer to Figures 3, 8 and 9.

Balanced Modulator

Figure 3 shows the MC1496 in a balanced modulator circuit operating with +12 and −8 volt supplies. Excellent gain and carrier suppression can be obtained with this circuit by operating the upper (carrier) differential amplifiers at a saturated level and the lower differential amplifier in a linear mode. The recommended input signal levels are 60 mV rms for the carrier and 300 mV rms for the maximum modulating signal levels.

For these input levels, the suppression of carrier, carrier harmonics, and sidebands of the carrier harmonics is given in Figures 4 and 5.

The modulating signal must be kept at a level to insure linear operation of lower differential amplifier Q5–Q6. If the signal input level is too high, harmonics of the modulating signal are generated and appear in the output as spurious sidebands of the suppressed carrier. For a maximum modulating signal input of 300 mV rms, the suppression of these spurious sidebands is typically 55 dB at a carrier frequency of 500 kHz.

Sideband output levels are shown in Figure 6 for various input levels of both carrier and modulating signal for the circuit of Figure 3.

Operating with a high level carrier input has the advantages of maximizing device gain and insuring that any amplitude variations present on the carrier do not appear on the output sidebands. It has the disadvantage of increasing some of the spurious signals.

Fourier analysis for a 50% duty cycle switching waveform at the carrier differential amplifiers predicts no even harmonics of the carrier (Appendix). However, the second harmonic of the carrier is suppressed only about 20 dB in the LF and HF range with a 60 mV carrier injection level, apparently due to factors such as the waveform not being a perfect square wave and slight mismatch between transistors. If the sine wave carrier signal is replaced with a 300 mV peak-to-peak square wave, an additional 15 dB of carrier, second-harmonic suppression is achieved. Attempting to accomplish the same result by increasing carrier sine-wave amplitude degrades carrier suppression due to additional carrier feedthrough with, however, no increase in the desired sideband output levels.

Operation with the carrier differential amplifiers in a linear mode theoretically should produce only the desired sidebands with no spurious outputs. Such linear operation is achieved by reducing the carrier input level to 15 mV rms or less.

This mode of operation does reduce spurious output levels significantly. Table 1 lists a number of the spurious output levels for high (60 mV) and low (10 mV) level carrier operation. Reduction of carrier injection from 60 mV to 10 mV decreased desired sideband output by 12.4 dB. This is in excellent agreement with the analysis in the Appendix, which predicts 12.5 dB.

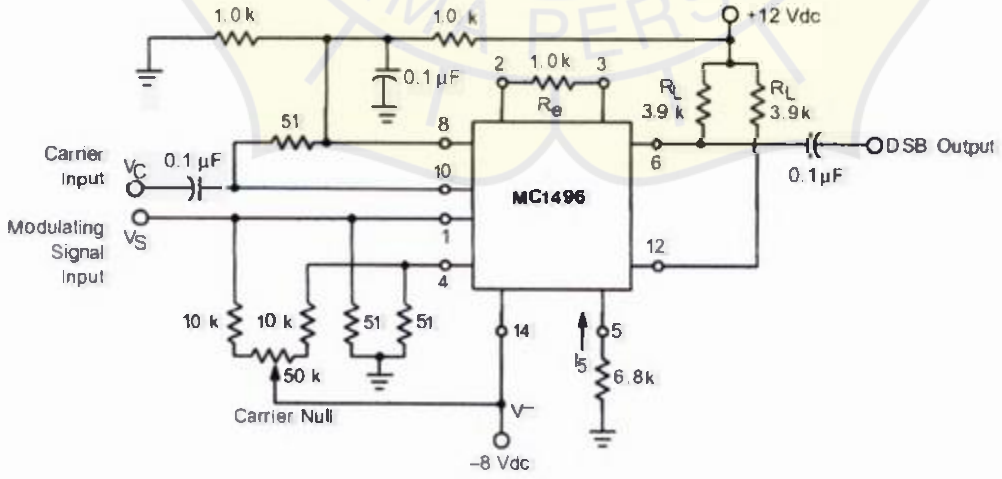

Figure 3. Balanced Modulator Circuit

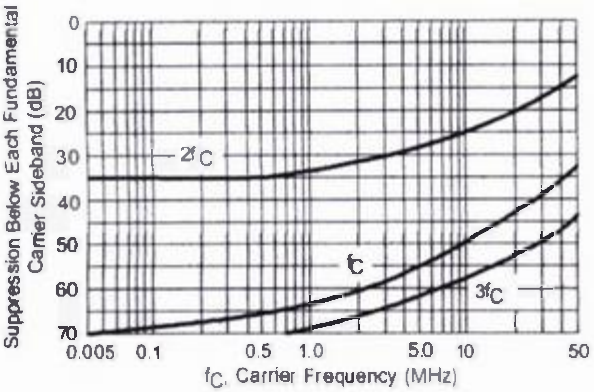

Figure 4. Balanced Modulator Carrier Suppression versus Frequency

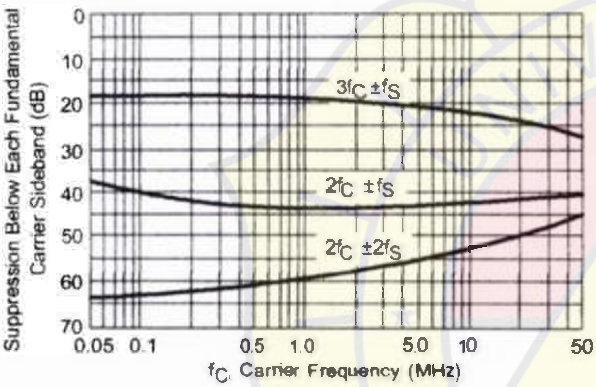

Figure 5. Balanced Modulator Suppression of Carrier Harmonic Sidebands versus Carrier Frequency

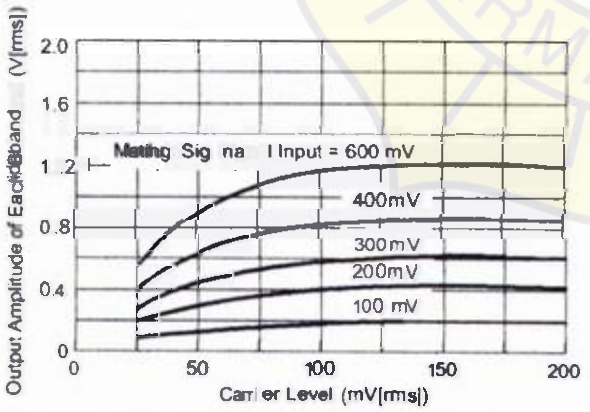

Figure 6. Balanced Modulator Sideband Output versus Carrier and Modulating Signal Inputs. Single Ended Operation.

Table 1. Suppression in dB of Spurious Outputs Below Each Desired Sideband ($f_C \pm f_S$) for High and Low Level Carrier Injection Voltages

	f_C	$2f_C$	$3f_C$	$2f_C \pm f_S$	$3f_C \pm f_S$
High Level Carrier Input 60 mV(rms)	66 dB	35 dB	70 dB	43 dB	19 dB
Low Level Carrier Input 10 mV(rms)	66 dB	45 dB	70 dB	53 dB	46 dB

Carrier Frequency = 500 kHz.
Modulating Signal = 1.0kHz at 300 mV(rms).
Circuit of Figure 3.

Spurious levels during low level operation are so low that they are affected significantly by the special purity of the carrier input signal. For example, initial readings for Table 1 were taken with a carrier signal generator which has second and third harmonics 42 and 45 dB below the fundamental, respectively. Additional filtering of the carrier input signal was required to measure the true second and third carrier–harmonic suppression of the MC1496.

The decision to operate with a low or high level carrier input would of course depend on the application. For a typical filter type SSB generator, the filter would remove all spurious outputs except some spurious sidebands of the carrier. For this reason operation with a high level carrier would probably be selected to maximize gain and insure that the desired sideband does not contain any spurious amplitude variations present on the carrier input signal.

On the other hand, in a low frequency broadband balanced modulator spurious outputs at any frequency may be undesirable and low level carrier operation may be the best choice.

Good carrier suppression over a wide temperature range requires low dc resistances between the bases of the lower differential amplifier (pins 1 and 4) and ground. It is recommended that the values of these resistors not be increased significantly higher than the 51 ohms utilized in the circuit shown in Figure 3 in applications where carrier suppression is important over full operating temperature range of −40°C to +125°C. Where operation is to be over a limited temperature range, resistance values of up to the low kilohm range may be used.

Amplitude Modulator

The MC1496 balanced modulator circuit shown in Figure 3 will function as an amplitude modulator with just one minor modification. All that is necessary is to unbalance the carrier null to insert the proper amount of carrier into the output signal. However, the null circuitry used for balanced modulator operation does not provide sufficient adjustment range and must be modified. The resulting amplitude modulator is shown in Figure 7. This modulator will provide excellent modulation at any percentage from zero to greater than 100 percent.

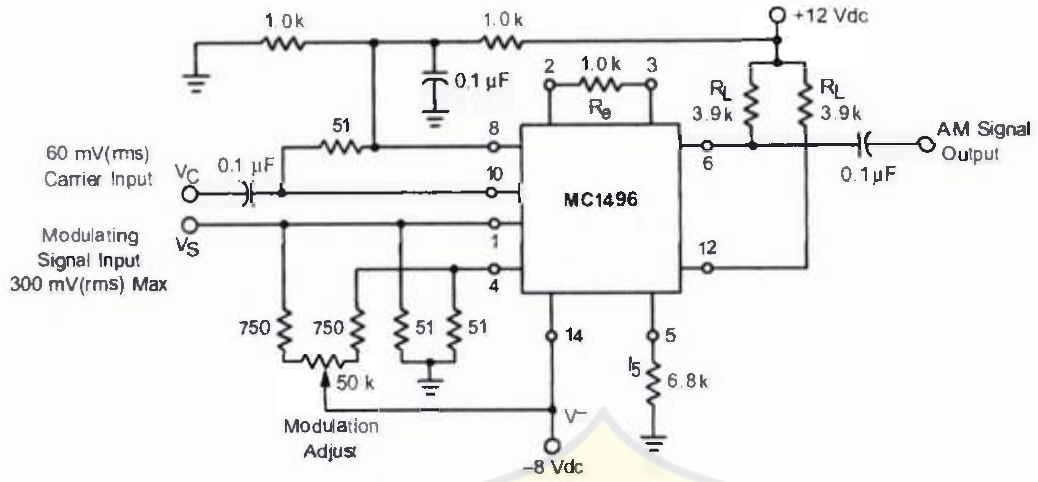

Figure 7. Amplitude Modulator

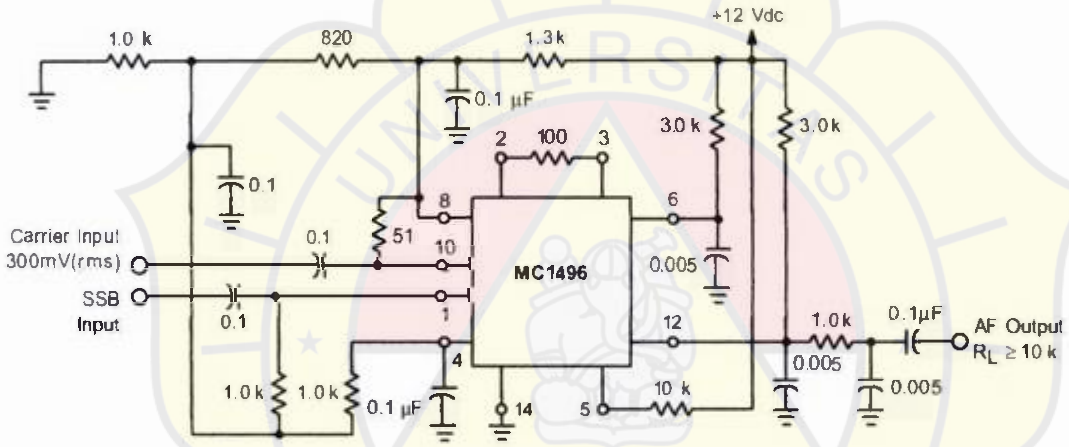

Figure 8. Product Detector +12 Vdc Single Supply

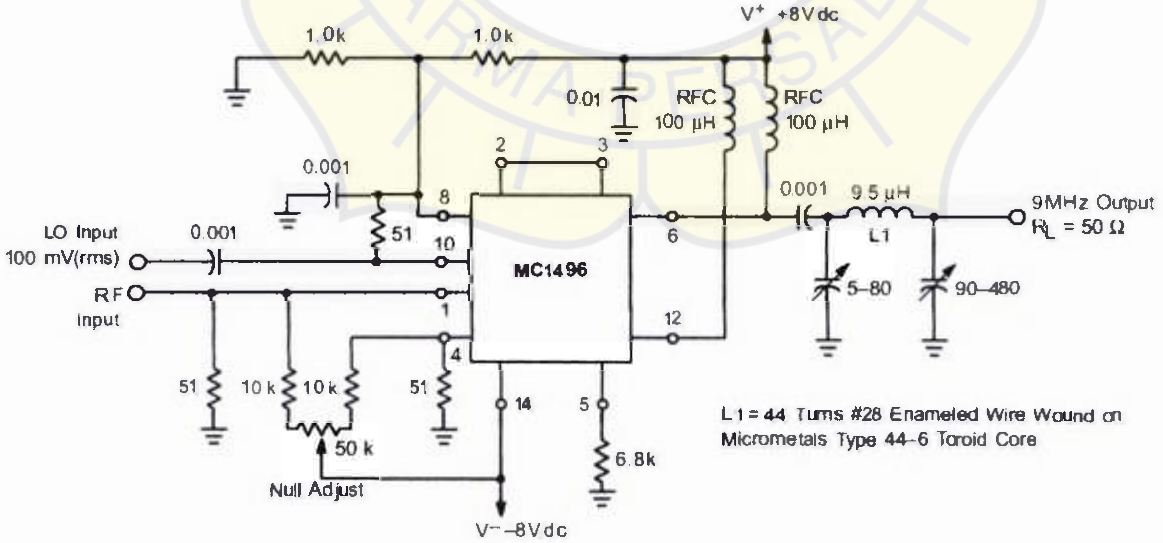

Figure 9. Double Balanced Mixer, Broadband Inputs, 9 MHz Tuned Output

Product Detector

Figure 8 shows the MC1496 in an SSB product detector configuration. For this application, all frequencies except the desired demodulated audio are in the RF spectrum and can be easily filtered in the output. As a result, the carrier null adjustment need not be included.

Upper differential amplifiers Q1–Q2 and Q3–Q4 are again driven with a high level signal. Since carrier output level is not important in this application (carrier is filtered in the output) carrier input level is not critical. A high level carrier input is desirable to maximize gain of the detector and to remove any carrier amplitude variations from the output. The circuit of Figure 8 performs well with a carrier input level of 100 to 500 mV rms.

The modulated signal (single–sideband, suppressed carrier) input level to differential amplifier pair Q5–Q6 is maintained within the limits of linear operation. Excellent linearity and undistorted audio output may be achieved with an SSB input signal level range up to 100 mV rms. Again, no transformers or tuned circuits are required for excellent product detector performance from very low frequencies up to 100 MHz.

Another advantage of the MC1496 product detector is its high sensitivity. The sensitivity of the product detector shown in Figure 8 for a 9 MHz SSB signal input and a 10 dB signal plus noise to noise [(S + N)/N] ratio at the output is 3 microvolts. For a 20 dB (S + N)/N ratio audio output signal it is 9 microvolts.

For a 20 dB (S + N)/N ratio, demodulated audio output signal, a 9 MHz SSB input signal power of - 101 dBm is required. As a result, when operated with an SSB receiver with a 50 ohm input impedance, a 0.5 microvolt RF input signal would require only 12 dB overall power gain from antenna input terminals to the MC1496 product detector.

Note also that dual outputs are available from the product detector, one from pin 6 and another from pin 12. One output can drive the receiver audio amplifiers while a separate output is available for the AGC system.

AM Detector

The product detector circuit of Figure 8 may also be used as an AM detector. The modulated signal is applied to the upper differential amplifiers while the carrier signal is applied to the lower differential amplifier.

Ideally, a constant amplitude carrier signal would be obtained by passing the modulated signal through a limiter ahead of the MC1496 carrier input terminals. However, if the upper input signal is at a high enough level (> 50 mV), its amplitude variations do not appear in the output signal. For this reason it is possible to use the product detector circuit shown in Figure 8 as an AM detector simply by applying the modulated signal to both inputs at a level of about 600 mV on modulation peaks without using a limiter ahead of the carrier input port. A small amount of distortion will be generated as the signal falls below 50 mV during modulation valleys, but it will probably not be significant in most applications. Advantages of the MC1496 AM detector include linear operation and the ability to have a detector stage with gain.

Mixer

Since the MC1496 generates an output signal consisting of the sum and difference frequencies of the two input signals only, it can also be used as a double balanced mixer.

Figure 9 shows the MC1496 used as a high frequency mixer with a broadband input and a tuned output at 9 MHz. The 3 dB bandwidth of the 9 MHz output tank is 450 kHz.

The local oscillator (LO) signal is injected at the upper input port with a level of 100 mV rms. The modulated signal is injected at the lower input port with a maximum level of about 15 mV rms. Note that for maximum conversion gain and sensitivity the external emitter resistance on the lower differential amplifier pair has been reduced to zero.

For a 30 MHz input signal and a 39MHz LO, the mixer has a conversion gain of 13 dB and an input signal sensitivity of 7.5 microvolts for a 10 dB (S + N)/N ratio in the 9 MHz output signal. With a signal input level of 20 mV, the highest spurious output signal was at 78 MHz (2 f_{LO}) and it was more than 30 dB below the desired 9 MHz output. All other spurious outputs were more than 50 dB down.

As the input is broadband, the mixer may be operated at any HF and VHF input frequencies. The same circuit was operated with a 200 MHz input signal and a 209 MHz LO. At this frequency the circuit had 9 dB conversion gain and a 14microvolt sensitivity.

Greater conversion gains can be achieved by using tuned circuits with impedance matching on the signal input port. Since the input impedance of the lower input port is considerably higher than 50 ohms even with zero emitter resistance, most of the signal input power in the broadband configuration shown is being dissipated in the 50 ohm resistor at the input port.

The circuit shown has the advantage of a broadband input with simplicity and reasonable conversion gain. If greater conversion gain is desired, impedance matching at the signal input is recommended.

The input impedance at the signal input port is plotted in Figures 10 and 11. The output impedance is also shown in Figure 12. Both of these curves indicate the complex impedance versus frequency for single ended operation.

The nulling circuit permits nulling of the LO signal and results in a few dB additional LO suppression in the mixer output. The nulling circuitry (the two 10 kΩ resistors and 50 kΩ potentiometer) may be eliminated when operating with a tuned output in many applications where the combination of inherent device balance and the output tank provide sufficient LO suppression.

The tuned output tank may be replaced with a resistive load to form a broadband input and output doubly balanced mixer. Magnitude of output load resistance becomes a simple matter of tradeoff between conversion gain and output signal bandwidth. As shown in Figure 12, the single ended output capacitance of the MC1496 at 9 MHz is typically 5 pF.

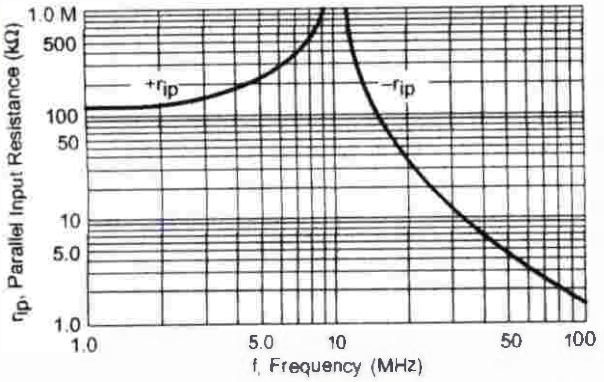

Figure 10. Signal–Port Parallel–Equivalent Input Resistance versus Frequency

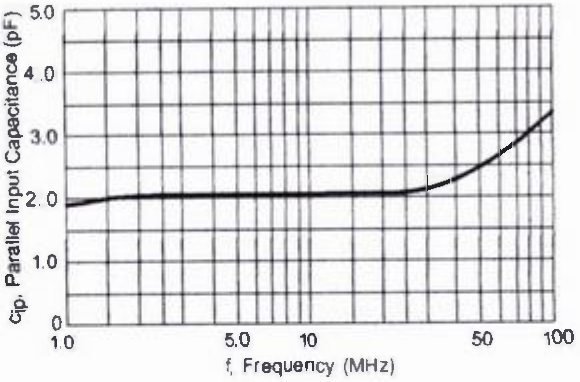

Figure 11. Signal–Port Parallel–Equivalent Input Capacitance versus Frequency

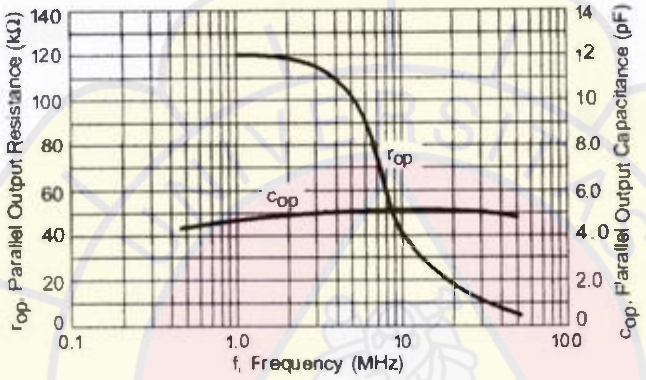

Figure 12. Single–Ended Output Impedance versus Frequency

With a 50 ohm output load, a 30 MHz input signal level of 20 mV, and 39 MHz LO signal level of 100 mV the conversion gain was –8.4 dB (loss). Isolation was 30 dB from input signal port to output port and 18 dB from LO signal port to output port.

Doubler

The MC1496 functions as a frequency doubler when the same signal is injected in both input ports. Since the output signal contains only $\omega_1 \pm \omega_2$ frequency components, there will be only a single output frequency at $2\omega_1$ when $\omega_1 = \omega_2$.

For operation as a broadband low frequency doubler, the balanced modulator circuit of Figure 3 need be modified only by adding ac coupling between the two input ports and reducing the lower differential amplifier emitter resistance between pins 2 and 3 to zero (tieing in 2 to pin 3). The latter modification increases the circuit sensitivity and doubler gain.

A low frequency doubler with these modifications is shown in Figure 13. This circuit will double in the audio and low frequency range below 1 MHz with all spurious outputs greater than 30 dB below the desired 2 f_{IN} output signal.

For optimum output–signal spectral purity, both upper and lower differential amplifiers should be operated within their linear ranges. This corresponds to a maximum input signal level of 15 mV rms for the circuit shown in Figure 13.

If greater signal handling capability is desired the circuit may be modified by using a 1000 ohm resistance between pins 2 and 3 and a 10:1 voltage divider to reduce the input signal at the upper port to 1/10 the signal level at the lower port.

The MC1496 will also function very well as an RF doubler at frequencies up to and including UHF. Either a broadband or a tuned output configuration may be used.

Suppression of spurious outputs is not as good at VHF and UHF. However, in the broadband configuration, the desired doubled output is still the highest magnitude output signal when doubling from 200 to 400 MHz, where the spurious outputs are 7 dB or more below the 400 MHz output. Even at this frequency the MC1496 is still superior to a conventional transistor doubler before output filtering.

Figure 14 shows a 150 to 300 MHz doubler with output filtering. All spurious outputs are 20 dB or more below the desired 300 MHz output.

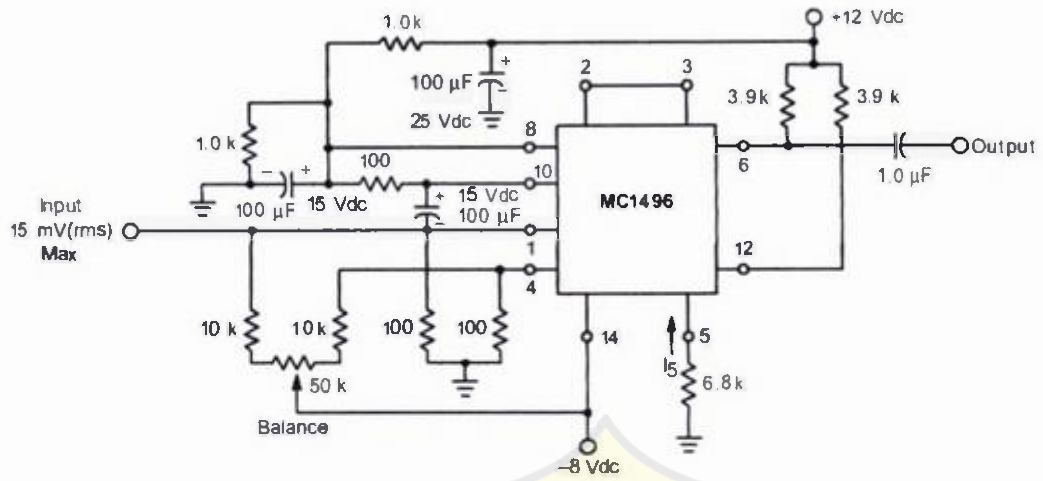

Figure 13. Low Frequency Doubler

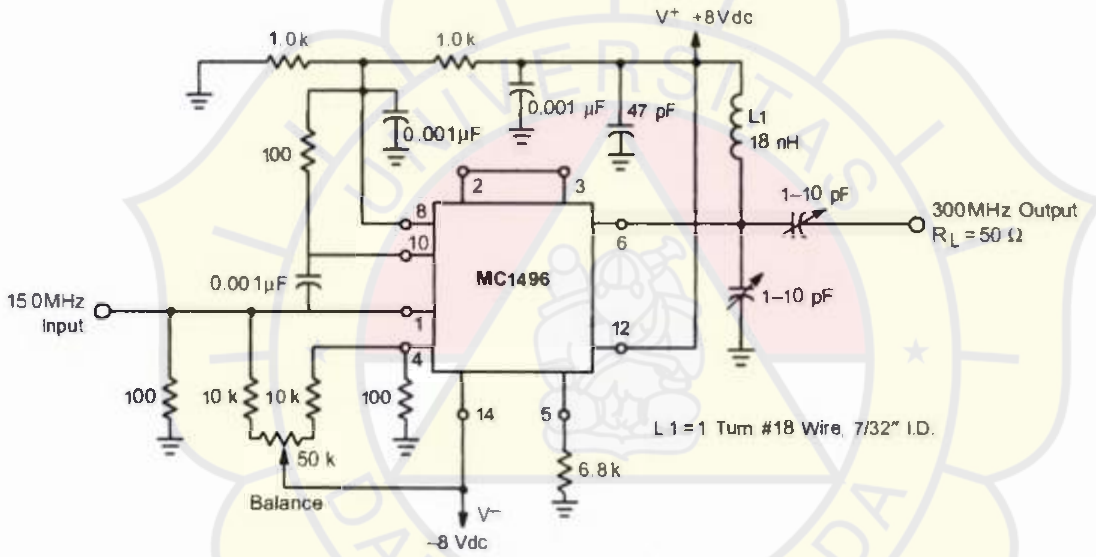

Figure 14. 150–300 MHz Doubler

FM Detector and Phase Detector

The MC1496 provides a dc output which is a function of the phase difference between two input signals of the same frequency, and can therefore be used as a phase detector. This characteristic can also be utilized to design an FM detector with the MC1496. All that is required is to provide a means by which the phase difference between the signals at the two input ports vary with the frequency of the FM signal.

Phase dependent FM detector operation can be explained by considering input and output currents for a high level signal at both input ports. These waveforms are shown in Figure 15 with inputs in phase at A and out of phase at B.

Since the output current is a constant times the product of the input currents, Figure 15 illustrates how a shift in phase between the two input signals causes a dc level shift in the output.

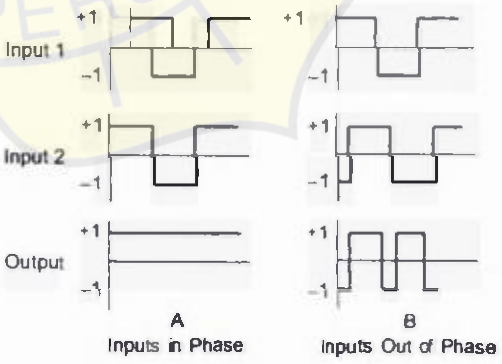

Figure 15. Phase Detector Waveforms, High Level Inputs

Summary

A number of applications of the MC1496 monolithic balanced modulator integrated circuit have been explored. The basic device characteristics of providing an output signal at the sum and difference of the two input frequencies with options on gain and amplitude characteristics will undoubtedly lead to numerous other applications not discussed in this article.

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APPENDIX

AC and DC Analysis

With reference in Figure 2 of the text, the following equations apply:

$$I_y = \frac{V_y}{R_E} \quad \text{(when } R_E \gg r_e\text{, the transistor dynamic emitter resistance.)} \tag{1A}$$

$$I_2 = \frac{I_1 + I_y}{1 + e^{\frac{V_x}{a}}}, \qquad I_3 = \frac{I_1 + I_y}{1 + e^{\frac{-V_x}{a}}}, \tag{2A}$$

$$I_4 = \frac{I_1 - I_y}{1 + e^{\frac{-V_x}{a}}}, \qquad I_5 = \frac{I_1 - I_y}{1 + e^{\frac{V_x}{a}}}$$

where

$$a = \frac{kT}{q} \tag{3A}$$

$$I_A = I_2 + I_4 = \frac{I_1 + I_y}{1 + e^{-m}} + \frac{I_1 - I_y}{1 + e^{m}} \tag{4A}$$

$$I_B = I_3 + I_5 = \frac{I_1 + I_y}{1 + e^{m}} + \frac{I_1 - I_y}{1 + e^{-m}}$$

where

$$m = \frac{V_x}{a}$$

$$I_A - I_B = (I_1 + I_y)\left[\frac{1}{1 + e^{m}} - \frac{1}{1 + e^{-m}}\right] \tag{5A}$$

$$+ (I_1 - I_y)\left[\frac{1}{1 + e^{m}} - \frac{1}{1 + e^{m}}\right]$$

$$= (I_1 - I_y)\left\{\frac{+ e^{-m} - 1 - e^{m}}{(1 + e^{m})(1 + e^{-m})}\right]$$

$$+ (I_1 - I_y)\left[\frac{1 + e^{m} \quad - 1 e^{-m}}{m)(1 e^{m})}\right]$$

$$= \frac{(I_1 + I_y)(e^{-m} - e^{m}) + (I_1 - I_y)(e^{m} - e^{-m})}{(1 + e^{m})(1 + e^{-m})}$$

$$= \frac{\left[\begin{array}{l} I_1 e^{-m} - I_1 e^{m} + I_y e^{-m} - I_y e^{m} \\ + I_1 e^{m} - I_1 e^{-m} - I_y e^{m} + I_y e^{-m} \end{array}\right]}{(1 + e^{m})(1 + e^{-m})}$$

$$= \frac{2I_y(e^{-m} - e^{m})}{(1 + e^{m})(1 + e^{-m})}$$

$$\Delta V_O = (I_A - I_B) R_L \tag{6A}$$

$$= \frac{2I_y R_L (e^{-m} - e^{m})}{(1 + e^{m})(1 + e^{-m})}$$

But,

$$I_y = \frac{V_{in}}{R_E} \tag{7A}$$

Therefore,

$$\frac{\Delta V_O}{V_{in}} = \frac{2R_L}{R_E}\left[\frac{e^{-m} - e^{m}}{(1 + e^{m})(1 + e^{-m})}\right] \tag{8A}$$

recalling that

$$m = \frac{V}{a} \quad \frac{x}{=} \quad \frac{V_x}{\frac{kT}{q}}$$

From this it can be seen that voltage gain is a function of the input level supplied to the upper four transistors:

$$\frac{\Delta V_O}{V_{in}} = A_V = \frac{2R_L}{R_E}[f(m)] \tag{9A}$$

and

$$V_O = \frac{2R_L V_y}{R_E}[f(m)] \tag{10A}$$

A curve of f(m) versus input level supplied to the upper quad differential amplifier is shown in Figure 16 of the text.

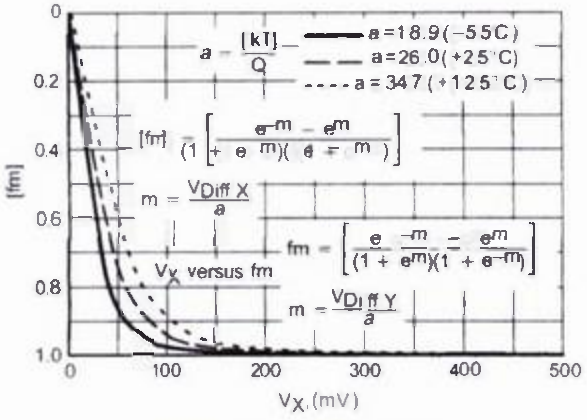


Figure 16. VX versus [fm]

The MC1496 is therefore a linear multiplier over the range of V_X for which [f(m)] is a linear function of V_X. This range of x can be obtained by inspection of Figure 16 and is approximately zero to 50 millivolts.

Examining the case of a small signal V_X input level mathematically yields:

Assume

$$V_X \ll a \tag{11A}$$

Then:

$$e^m \leq 0.1 \tag{12A}$$

$$e^m \approx 1 + m \tag{13A}$$

$$e^{-m} \approx 1 - m$$

$$[f(m)] \approx \left[\frac{(1-m)-(1+m)}{(2+m)(2-m)}\right] = \left(\frac{-2m}{4-m^2}\right) \tag{14A}$$

$$\left(\frac{-2m}{4-m^2}\right) \approx \frac{-2}{4}m = \frac{-m}{2} \tag{15A}$$

Therefore

$$A_V = \frac{V_O}{V_y} = \frac{2R_L}{R_E}\left(\frac{(-m)}{2}\right) = \frac{-R_L m}{R_E} \tag{16A}$$

$$V_O = \frac{-R_L V_y m}{R_E} = \frac{-R_L V_y V_x}{R_E a} \tag{17A}$$

Equation (17A) shows that the MC1496 is a linear multiplier when $V_X \leq 2.6$ mV. However, as was observed by inspection of Figure 16 earlier, the device is capable of approximate linear multiplier operation when $V_X \leq 50$ mV.

For the case of a large signal V_X input level:

$$V_X \gg a \tag{18A}$$

$$e^m \gg 1 \tag{19A}$$

$$e^{-m} \ll 1$$

$$A_V = \frac{2R_L}{R_E}\left[\frac{-e^m}{e^m}\right] = \frac{-2R_L}{R_E} \tag{20A}$$

$$V_O = \frac{-2R_L V_y}{R_E} \tag{21A}$$

Equation (20A) indicates that in this mode the output level is independent of the level of V_X. This characteristic is useful in many communications applications of the MC1496.

Mathematical analysis for ac input signals is given below for two modes of operation which cover most applications of the MC1496. These modes are (1) V_x and V_y both low level sine waves, and (2) low level sine wave for V_y and a large signal input for V_x (either a high level sine wave or a square wave input) giving rise to a symmetrical switching operation of the upper differential amplifier quad, Q1, Q2, Q3, and Q4.

For sine wave input signals,

$$V_x = E_x \cos\omega_x t \tag{22A}$$

$$V_y = E_y \cos\omega_y t \tag{23A}$$

where E_x and E_y are the peak values of the x and y input voltages, respectively. Therefore,

$$V_O = KE_xE_y(\cos\omega_x t)(\cos\omega_y t) \tag{24A}$$

Performing this multiplication yields:

$$V_O = \frac{KE_xE_y}{2}\cos(\omega_x + \omega_y)t + \cos(\omega_x - \omega_y)t \tag{25A}$$

The second mode of operation can be analyzed by assuming square wave switching function in the upper differential amplifiers and applying Fourier analysis.

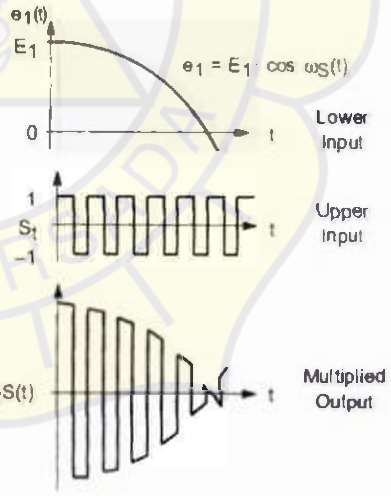


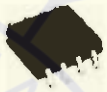
Figure 17. Input and Output Waveforms for a High Level Upper Input and Low Level Input Signals

UA741

GENERAL PURPOSE SINGLE OPERATIONAL AMPLIFIER

- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGHGAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION
- REQUIRED
- SAME PIN CONFIGURATION AS THE UA709

N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The UA741 is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intented for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

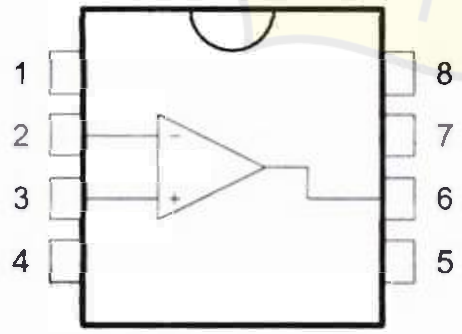
The high gain and wide range of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/ octave) insures stability in closed loop circuits.

ORDER CODE

Part Number	Temperature Range	Package	
		N	D
UA741C	0°C, +70°C	•	•
UA741I	-40°C, +105°C	•	•
UA741M	-55°C, +125°C	•	•
Example : UA741CN			

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)



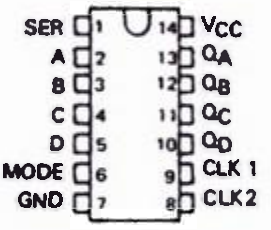
1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SN5495A, SN54LS95B
SN7495A, SN74LS95B
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

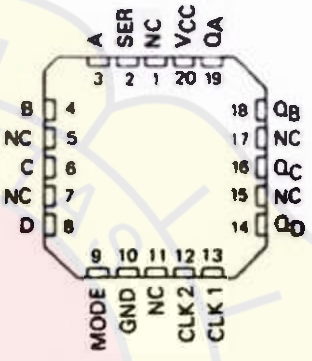
SDLS128 – MARCH 1974 – REVISED MARCH 1988

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'LS95B	36 MHz	85 mW

SN5495A, SN54LS95B . . . J OR W PACKAGE
SN7495A . . . N PACKAGE
SN74LS95B . . . D OR N PACKAGE
(TOP VIEW)



SN54LS95B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

FUNCTION TABLE

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

TEXAS INSTRUMENTS
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