BAB V

KESIMPULAN

Selama dalam proses pembuatan sampai dengan tahap pengujian maka dapat diambil beberapa kesimpulan antara lain:

Dari hasil pengujian IC MT 8870 cukup baik digunakan untuk mendeteksi sinyal tone dekoder dari penggunaan IC LM 567 PLL.

Alat ini diharapkan dapat dikembangkan lebih lanjut dengan menambah data base atau mengembangkan software sehingga dapat mencakup seluruh kota di Indonesia dan Internasional kemudian menggantikan komputer dengan sebuah prossesor sehingga alat penghitung biaya pulsa telepon ini dapat dalam suatu kotak kecil.

```
rocedure Deteksi_key;
ype
    DigitTelp = ARRAY[1..11] Of String;

  record_SLJJ = RECORD
                    Kode    : String[5];
                    Kota    : string[25];
                    tarif   : string[10];
                    end;
  Tipe_File_SLJJ = FILE of record_SLJJ;
ar
   No_Telp : DigitTelp;
   Ulang,Bit_Telepon  : Integer;
   X: Longint;
   No_Telp_Byte ,Nada_Panggil,Detek,Trans: byte;
   SLJJ,No_Telp_Str,Data_Tarif : String;

File_SLJJ : File of Record_SLJJ;
Data_SLJJ : Record_SLJJ;
Data_Kode,Data_Kota : string;
Y    : string;
I Tampil2.inc}
I Tampil3.Inc}
ocedure ubah_NoTelp_KeString(Var No_Telp_Byte:byte;
                             Var No_Telp_Str :String);
egin
SE No_Telp_Byte Of

: Begin
      Bit_Telepon:=1;
      str(Bit_Telepon,No_Telp_Str);
   End;
: Begin
      Bit_Telepon:=2;
      str(Bit_Telepon,No_Telp_Str);
   End;
: Begin
      Bit_Telepon:=3;
      str(Bit_Telepon,No_Telp_Str);
   End;
  Begin
      Bit_Telepon:=4;
      str(Bit_Telepon,No_Telp_Str);
   End;
  Begin
      Bit_Telepon:=5;
      str(Bit_Telepon,No_Telp_Str);
   End;
  Begin
      Bit_Telepon:=6;
      str(Bit_Telepon,No_Telp_Str);
   End;
Begin
      Bit_telepon:=7;
      str(Bit_Telepon,No_Telp_Str);
```

```
    End;
3: Begin
        Bit_Telepon:=8;
        str(Bit_Telepon,No_Telp_Str);
    End;
9: Begin
        Bit_Telepon:=9;
        str(Bit_Telepon,No_Telp_Str);
    End;
0 : Begin
        Bit_Telepon:=0;
        str(Bit_Telepon,No_Telp_Str);
    End;
nd;
nd;

**** Program Utama ****)
egin
o_Telp[1]:='';
o_Telp[2]:='';
o_Telp[3]:='';
o_Telp[4]:='';
o_Telp[5]:='';
o_Telp[6]:='';
o_Telp[7]:='';
o_Telp[8]:='';
o_Telp[9]:='';
o_Telp[10]:='';
o_Telp[11]:='';
ang:=0;
epeat
 Repeat
   Detek:=MEM[$A000:0002];
 Until (Detek=$8) or (Detek=$1);

o_Telp_Byte:=MEM[$A000:0001];
f Detek=$8 Then
 Begin
  Ulang:=Ulang+1;
  ubah_NoTelp_Kestring(No_Telp_Byte,No_telp_str);
  No_Telp[Ulang]:=No_Telp_str;
  Gotoxy(1+ulang,2); write(No_Telp[Ulang]);
 End;

 Repeat
  Detek:=MEM[$A000:0002];
 Until (Detek=$0) or (Detek=$1);

til (Detek=$1);

toXY(1,2); DelLine;

epeat Until Keypressed;}
**********************************)
 No_Telp[1]='0' Then
```

```
  Begin
   SLJJ:=Concat(No_Telp[1],No_Telp[2],No_Telp[3]);
    If (SLJJ='021') or (SLJJ='022') or (SLJJ='024') or
       (SLJJ='031') or (SLJJ='066') Then
       Begin
         (*************************************************************

         Gotoxy(1,7);Write('Nomor Yang Dituju :', No_Telp[4],No_Telp[5
p[6],No_Telp[7],
                    No_Telp[8],No_Telp[9],No_Telp[10],No_Telp[11]);
         assign(File_SLJJ,'SLJJ.DTA');
         Reset(File_SLJJ);
         while Data_kode<>SLJJ  Do
          with Data_SLJJ DO
            Begin
             Read(File_SLJJ,Data_SLJJ); {Membaca file}
             Data_Kode:=Data_SLJJ.Kode;
             Data_Kota:=Data_SLJJ.Kota;
             Data_tarif:=Data_SLJJ.Tarif;
             end;
           Gotoxy(1,4);write('  Kode SLJJ :',Data_kode);
           Gotoxy(1,5);write('Kota tujuan :',Data_Kota);
           Gotoxy(1,6);write('      Pulsa :',Data_Tarif,' Detik per Pu

(************************ AKhir Data base SLJJ*********)
          If Detek=$1 Then
          Begin
           waktu3(Data_Tarif);
          end;
       End
     Else
     Begin
       SLJJ:=Concat(No_Telp[1],No_Telp[2],No_Telp[3],No_Telp[4]);
       Gotoxy(1,7);Write('Nomor Yang Dituju :', No_Telp[5],No_Telp[6]
],
                    No_Telp[8],No_Telp[9],No_Telp[10],No_Telp[11]);
         assign(File_SLJJ,'SLJJ.DTA');
         Reset(File_SLJJ);
         while Data_kode<>SLJJ  Do
          with Data_SLJJ DO
            Begin
             Read(File_SLJJ,Data_SLJJ); {Membaca file}
             Data_Kode:=Data_SLJJ.Kode;
             Data_Kota:=Data_SLJJ.Kota;
             Data_tarif:=Data_SLJJ.Tarif;
            end;
           Gotoxy(1,4);write('  Kode SLJJ :',Data_kode);
           Gotoxy(1,5);write('Kota tujuan :',Data_Kota);
           Gotoxy(1,6);write('      Pulsa :',Data_Tarif,' Detik per Pu

      If Detek=$1 Then
      Begin
       waktu3(Data_Tarif);
      End;
     End;
  end
lse
egin
Gotoxy(1,7);Write('Nomor Yang Dituju :', No_Telp[1],No_Telp[2],No_Tel

                    No_Telp[4],No_Telp[5],No_Telp[6],No_Telp[7]);
```

```
:f Detek=$1 Then
iegin
 waktu2;
:nd;
:nd;
 ***************************************)
:nd;
```

```
rocedure Waktu2;
ar Selisih_Jumlah,Jumlah1,Jumlah2 : longint;
   Data_Display ,display,Data_word,Data_word2,Data_word3,
   Data_word4,Data_word5: longint;
   Data_str,data_str1,Data_str2,Data_str3,Data_str4,Data_str5,
   Selisih_Jumlah_str : String;
   Data_Integer ,y,Pulsa: longint;
   x,Pembagi:Integer;
   Deteksi_OffHook : Byte;
rocedure TulisJam1;
ar awalX,awalY : Byte;
   Jam,Menit,Detik,Detik_100,Sem : Word;
   Recwaktu : DateTime;
   Waktu    : longint;
egin
TTIME(Jam,Menit,Detik,Detik_100);
 Sem <> Detik Then
  Begin
    Sem := detik;
  End;
mlah1:=Jam*3600 + Menit*60 + Detik;
d;

ocedure TulisJam2;
r awalX,awalY : Byte;
   Jam,Menit,Detik,Detik_100,Sem : Word;
   Recwaktu : DateTime;
   Waktu    : longint;
gin
TTIME(Jam,Menit,Detik,Detik_100);
 Sem <> Detik Then
 Begin
   Sem := detik;
 End;
lah2:=Jam*3600 + Menit*60 + Detik;
;


cedure Bit_Display(Var Data_str:string);
in
(Data_str,Data_integer,x);
E Data_Integer of
 Begin
      MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$00;
  End;
 Begin
      MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$10;
  End;
 Begin
      MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$20;
  End;
 Begin
      MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$30;
  End;
 Begin
```

```
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$40;
    End;
 : Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$50;
    End;
 : Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$60;
    End;
': Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$70;
    End;
]: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$80;
    End;
': Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$90;
    End;
nd;
nd;

**********************************************************)

rocedure Bit_Display2(Var Data_str2:string);
egin
al(Data_str2,Data_word2,x);
ASE Data_word2 of
 : Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$00;
    End;
 : Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$10;
    End;
 : Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$20;
    End;
 : Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$30;
    End;
 : Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$40;
    End;
 : Begin
       MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$50;
    End;
 : Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$60;
    End;
 Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$70;
    End;
 Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$80;
    End;
 Begin
        MEM[$A000:$0000]:=$F7;MEM[$A000:$0002]:=$90;
```

```
   End;
d;
d;

*****************************************)

ocedure Bit_Display3(Var Data_str3:string);
gin
l(Data_str3,Data_word3,x);
SE Data_word3 of

: Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$00;
   End;
: Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$10;
   End;
 Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$20;
   End;
 Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$30;
   End;
 Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$40;
   End;
 Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$50;
   End;
 Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$60;
   End;
Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$70;
   End;
Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$80;
   End;
Begin
      MEM[$A000:$0000]:=$FB;MEM[$A000:$0002]:=$90;
   End;

*****************************************)
edure Bit_Display4(Var Data_str4:string);
n
Data_str4,Data_word4,x);
 Data_word4 of

Begin
      MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$00;
   End;
Begin
      MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$10;
   End;
```

```
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$20;
    End;
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$30;
    End;
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$40;
    End;
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$50;
    End;
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$60;
    End;
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$70;
    End;
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$80;
    End;
: Begin
        MEM[$A000:$0000]:=$FD;MEM[$A000:$0002]:=$90;
    End;
nd;
nd;
**************************************************)

rocedure Bit_Display5(Var Data_str:string);
gin
l(Data_str,Data_word,x);
SE Data_word of
: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$00;
    End;
: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$10;
    End;
: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$20;
    End;
: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$30;
    End;
: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$40;
    End;
  Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$50;
    End;
  Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$60;
    End;
Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$70;
```

```
    End;
: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$80;
    End;
: Begin
        MEM[$A000:$0000]:=$EF;MEM[$A000:$0002]:=$90;
    End;
nd;
nd;

**************************************************)

egin
EM[$A000:$0003]:=$83;  { Inisialisasi 8255 }
embagi:=18;  (********** Variabel Pulsa *******)
clrscr;}
ulisJam1;

epeat
ulisJam2;
Pulsa:=Jumlah2-Jumlah1;
Selisih_Jumlah:=11*(Pulsa div Pembagi);
Str(Selisih_Jumlah,Selisih_Jumlah_str);
f Selisih_Jumlah<10 Then
egin
f Selisih_Jumlah<10 Then
  Begin
    Data_str1:=copy(Selisih_Jumlah_str,1,1);
    Bit_Display(Data_str1);
  End
  Else
 If Selisih_Jumlah>=9 Then
  Begin
    Data_str1:=copy(Selisih_Jumlah_str,2,1);
    Bit_Display(Data_str1);
  End
  Else
  If Selisih_Jumlah>99 Then
   Begin
    Data_str1:=copy(Selisih_Jumlah_str,3,1);
    Bit_Display(Data_str1);
   End
   Else
   If Selisih_Jumlah>999 Then
    Begin
     Data_str1:=copy(Selisih_Jumlah_str,4,1);
     Bit_Display(Data_str1);
    End
    Else
      Begin
       Data_str1:=copy(Selisih_Jumlah_str,5,1);
       Bit_Display(Data_str1);
      End;
nd;
*********************************************)
```

```
If (Selisih_Jumlah>9) and (Selisih_Jumlah<100)Then
   Begin
    Data_str1:=copy(Selisih_Jumlah_str,2,1);
    Bit_Display(Data_str1);
    Data_str2:=copy(Selisih_Jumlah_Str,1,1);
    Bit_display2(Data_str2);
   End
 Else
 If (Selisih_Jumlah>99) and (Selisih_Jumlah<1000) Then
    Begin
     Data_str1:=copy(Selisih_Jumlah_str,3,1);
     Bit_Display(Data_str1);
     Data_str2:=copy(Selisih_Jumlah_Str,2,1);
     Bit_display2(Data_str2);
     Data_str3:=copy(Selisih_Jumlah_Str,1,1);
     Bit_display3(Data_str3);
    End
   Else
   If (Selisih_Jumlah>999) And (Selisih_Jumlah<10000) Then
    Begin
     Data_str1:=copy(Selisih_Jumlah_str,4,1);
     Bit_Display(Data_str1);
     Data_str2:=copy(Selisih_Jumlah_Str,3,1);
     Bit_display2(Data_str2);
     Data_str3:=copy(Selisih_Jumlah_Str,2,1);
     Bit_display3(Data_str3);
     Data_str4:=copy(Selisih_Jumlah_Str,1,1);
     Bit_display4(Data_str4);
    End
    Else
    If Selisih_Jumlah>9999 Then
    Begin
     Data_str1:=copy(Selisih_Jumlah_str,5,1);
     Bit_Display(Data_str1);
     Data_str2:=copy(Selisih_Jumlah_Str,4,1);
     Bit_display2(Data_str2);
     Data_str3:=copy(Selisih_Jumlah_Str,3,1);
     Bit_display3(Data_str3);
     Data_str4:=copy(Selisih_Jumlah_Str,2,1);
     Bit_display4(Data_str4);
     Data_str5:=copy(Selisih_Jumlah_Str,1,1);
     Bit_display5(Data_str5);
    End;
oxy(1,12); writeln('Lama Pembicaraan :',Pulsa,' Detik');
oxy(1,13); writeln('          Biaya :',Selisih_Jumlah ,' Rupiah');
eteksi_OffHook:=MEM[$A000:0001];
eteksi_offHook:= Deteksi_OffHook And $80;
il Deteksi_OffHook=$80;
;
```

MOTOROLA

MC14543B

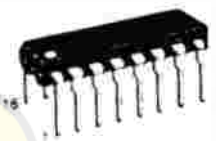
BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).
- Chip Complexity: 207 FETs or 52 Equivalent Gates

L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = −55 to 125 C for all packages

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Input Current per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−55 to +125	°C
Power Dissipation, per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} / I_{OLmax}	10	mA
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} / P_{OLmax}	70	mW

*$P_{Dmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

TRUTH TABLE

INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	0	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	0	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	†					Invert Above Output Combinations							Display as Above

X = Don't care
* = Above Combinations
† = For LC readouts, apply 50 Hz to 4 kHz square wave to Ph
For common cathode LED readouts, select Ph = 0
For common anode LED readouts, select Ph = 1
** = Depends upon the BCD code previously entered while LD = 1

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ#	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	—	—	—	−10.1	—	—	—	
(V_{OH} = 13.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 9.5 Vdc)		10	—	—	—	10.1	—	—	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.1 μA/kHz) f + I_{DD}							
		15	I_T = (4.7 μA/kHz) f + I_{DD}							

Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3}(C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

†The formulas given are for the typical characteristics only at 25°C.

MITEL

ISO2-CMOS MT8870C/MT8870C-1
Integrated DTMF Receiver

9161-002-051-NA ISSUE 3 December 1988

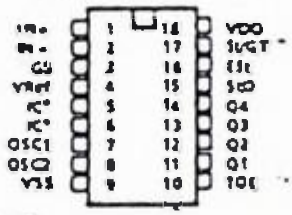
Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870B-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers

Pin Connections



* Connected to VSS

Ordering Information

MT8870C/MT8870C-1 Plastic DIP
MT8870C/MT8870C-1 Cerdip
-40°C to +85°C

Description

The MT8870C/MT8870C-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO2-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

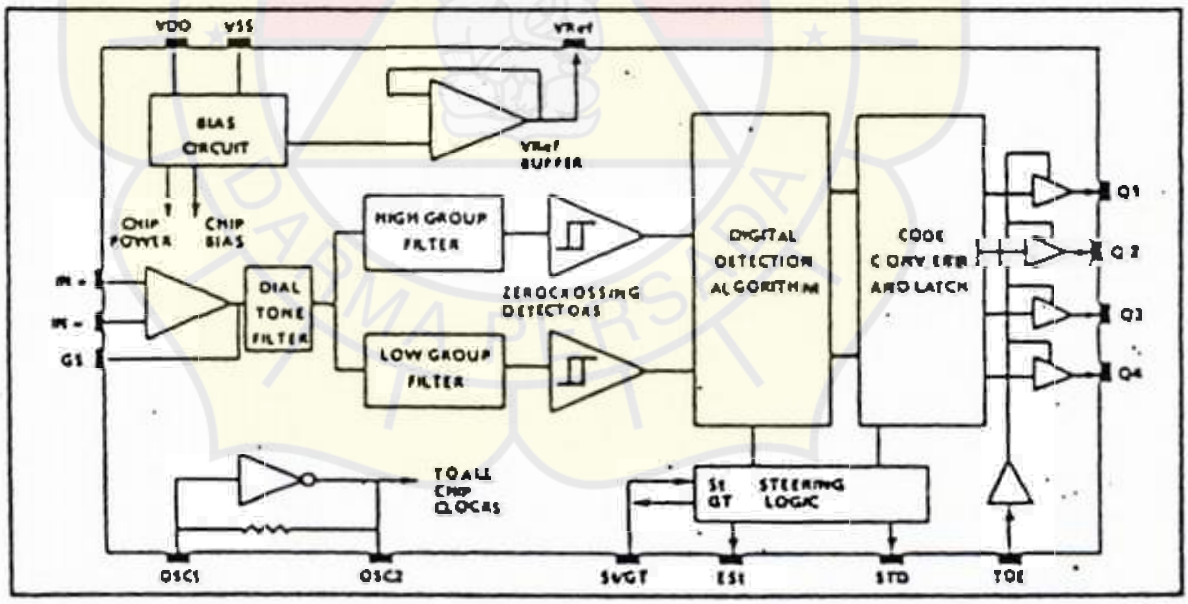


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}			6	V
2	Voltage on any pin		V_{SS} -0.3	V_{DD}+0.3	V
3	Current at any pin(other than supply)			10	mA
4	Operating temperature	T_A	-40	+85	°C
5	Storage temperature		-65	+150	°C
6	Package power dissipation			1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 14mW/°C. All leads soldered to board

Recommended Operating Conditions- Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1		Positive Supply Voltages	V_{DD}		5		V	V_{SS} = 0V
2		Oscillator Clock Frequency	fc		3.579545		MHz	
3		Oscillator Frequency Tolerance	Δfc		±0.1		%	

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics- V_{DD} = 5.0V ± 5%, V_{SS} = 0V voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	SUPPLY	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_D		15	45	mW	f @ 3.58 MHz; V_{DD} = 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5		Low level input voltage	V_{IL}			1.5	V	
6		Input leakage current	I_{IH}/I_{IL}		0.1		µA	V_{IN} = V_{SS} or V_{DD}
7		Pull-up(source) current	I_{SO}		7.5	15	µA	TOE (pin 10) = 0V
8		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1kHz
9		Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			V_{SS} +0.03	V	No load
11		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
12		Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} =0.4V
13		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
14		V_{Ref} output voltage	V_{Ref}	2.4		2.7	V	No load
15		V_{Ref} output resistance	R_{OR}		10		kΩ	

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

Operating Characteristics[1] - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ[‡]	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power supply rejection	PSRR		60		dB	1KHz
5	Common mode rejection	CMRR		60		dB	$-3.0V \le V_{IN} \le 3.0V$
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_C		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \ge 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		KΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

[‡] $V_{DD} = 5V$, $V_{SS} = 0V$, $T_A = 25°C$

[1] [illegible] design aid only; not guaranteed and not subject to production testing

MT8870B AC Electrical Characteristics[1] - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mV_{RMS}	1,2,3,5,6,9
2		Positive twist accept			10		dB	2,3,6,9
3		Negative twist accept			10		dB	2,3,6,9
4		Freq. deviation accept		±1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject		±3.5%			Nom.	2,3,5,9
6		Third tone tolerance			-16		dB	2,3,4,5,9
7		Noise tolerance			-12		dB	2,3,4,5,7,9,10
6		Dialtone tolerance			+22		dB	2,3,4,5,8,9,11

[‡] $V_{DD} = 5V$, $V_{SS} = 0$, $T_A = 25°C$, [illegible] 3.579545MHz [illegible] using test circuit shown in Figure 2

NOTES

1. dBm = decibels above or below a reference power of 1mW into a 600 ohm load
2. [illegible] sequence [illegible] of [illegible] tones
3. [illegible] tone [illegible]
4. Signal condition consists of nominal DTMF frequencies
5. [illegible]
6. [illegible] tone [illegible] ±1.5% ± 2Hz
7. Bandwidth limited [illegible] Gaussian noise
8. The precise dial tone frequencies are [illegible] Hz and 440 Hz ± 2%
9. For an error rate of better than 1 in 10,000
10. Referenced to lowest level frequency component in DTMF signal
11. [illegible]

AC Electrical Characteristics — voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ[4]	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	$t_{\overline{ID}}$	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PSTD}		12		µs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QSTD}		3.4		µs	TOE = V_{DD}
10		Propagation delay (TOE to QENABLE)	t_{PTE}		50		ns	RL = 10KΩ CL = 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	RL = 10KΩ CL = 50 pF
12	CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
13		Clock input rise time	t_{rCL}			110	ns	Ext. clock
14		Clock input fall time	t_{fCL}			110	ns	Ext. clock
15		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
16		Capacitive load (OSC2)	C_{LO}			30	pF	

[3] V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25°C and f_C = 3.5795 MHz, using test circuit shown in Figure 2.
[4] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

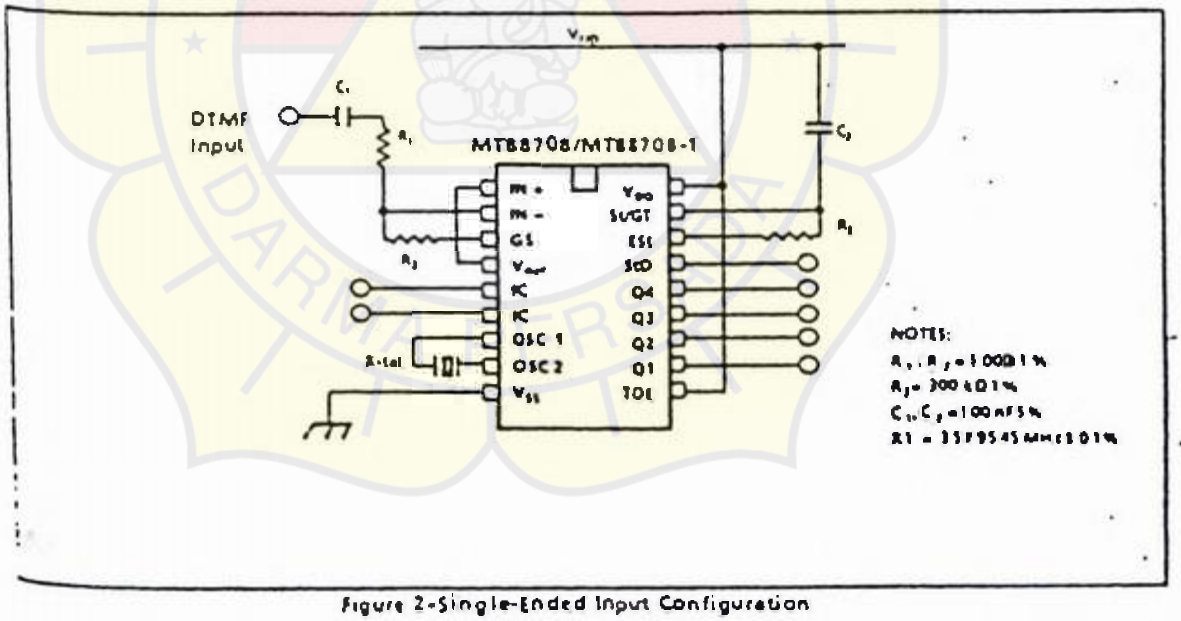


Figure 2-Single-Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN+	Non-Inverting Op-Amp (Input).
2	IN-	Inverting Op-Amp (Input).
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{Ref}	Reference Voltage (Output). Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig.2).
5	IC	Internal Connection. Must be tied to V_{SS}.
6	IC	Internal Connection. Must be tied to V_{SS}.
7	OSC1	Clock (Input).
8	OSC2	Clock (Output). A 3.579545MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative Power Supply (Input).
10	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
16	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply (Input).

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '00, '04, '10, '20, '30			SERIES 54H / SERIES 74H '100, '104, '110, '120, '130			SERIES 54L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS / SERIES 74LS 'L500, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S / SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.1	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25				4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−500			−100			−400			−1000	μA
	74 Family			−400			−500						−400			−1000	
Low-level output current, I_{OL}	54 Family			16			20			2			4			20	mA
	74 Family			16			20						8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70				0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS[1]			SERIES 54 / SERIES 74 '00, '04, '10, '20, '30			SERIES 54H / SERIES 74H '100, '104, '110, '120, '130			SERIES 54L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS / SERIES 74LS 'L500, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S / SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
						MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.8			0.8	V
					74 Family			0.8			0.8						0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = −12 mA					−1.5			−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.5					2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4					0.25	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS												0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1			0.1						1	mA
					V_I = 7 V												0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50			10							μA
					V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.3 V									−0.18							mA
					V_{IL} = 0.4 V			−1.6			−2						−0.4				
					V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current[3]	6	V_{CC} = MAX		54 Family	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
					74 Family	−18		−55	−40		−100				−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page															mA

supply current†

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'00	4	8	12	22	2
'04	8	12	18	33	2
'10	3	6	9	16.5	2
'20	2	4	6	11	2
'30	1	2	3	6	2
'H00	10	18.8	26	40	4.5
'H04	16	26	40	58	4.5
'H10	7.5	12.6	19.5	30	4.5
'H20	5	8.4	13	20	4.5
'H30	2.5	4.2	6.5	10	4.5
'L00	0.44	0.8	1.16	2.04	0.20
'L04	0.66	1.2	1.74	3.06	0.20
'L10	0.33	0.6	0.87	1.53	0.20
'L20	0.22	0.4	0.58	1.02	0.20
SN54L30	0.11	0.22	0.29	0.51	0.20
'LS00	0.8	1.6	2.4	4.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4
'LS10	0.6	1.2	1.8	3.3	0.4
'LS20	0.4	0.8	1.2	2.2	0.4
'LS30	0.35	0.5	0.6	1.1	0.48
'500	10	18	20	34	3.75
'504	15	24	30	54	3.75
'510	7.5	12	15	27	3.75
'520	5	8	10	18	3.75
'530	3	5	5.5	10	4.25
'S133	3	5	5.5	10	4.25

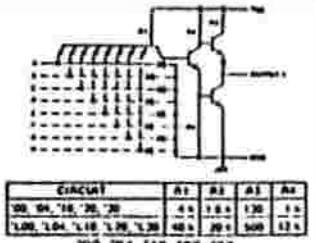
†Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS‡	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C_L = 15 pF, R_L = 400 Ω		11	22		7	15
'04, '20			12	22		8	15
'30			13	22		8	15
'H00	C_L = 25 pF, R_L = 280 Ω		5.9	10		6.2	10
'H04			6	10		6.6	10
'H10			5.9	10		6.2	10
'H20			6	10		7	10
'H30			6.6	10		8.9	12
'L00, 'L04, 'L10, L20	C_L = 50 pF, R_L = 4 kΩ		35	60		31	60
'L30			35	60		70	100
'LS00, 'LS04, 'LS10, 'LS20	C_L = 15 pF, R_L = 2 kΩ		9	15		10	15
'LS30			9	15		13	20
'500, '504	C_L = 15 pF, R_L = 280 Ω		5	4.5		3	5
'510, '520	C_L = 50 pF, R_L = 280 Ω		4.5			5	
'530, 'S133	C_L = 15 pF, R_L = 280 Ω		4	5		4.5	7
	C_L = 50 pF, R_L = 280 Ω		5.5			6.5	

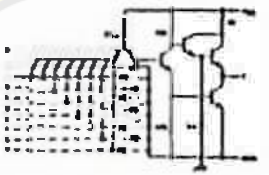
‡Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)

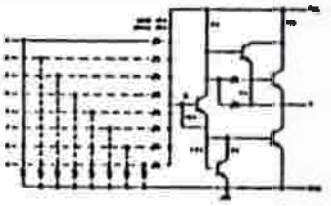


CIRCUIT	A1	A2	A3	A4
'00, '04, '10, '20, '30	4 k	1.6 k	130	1 k
'L00, 'L04, 'L10, 'L20, 'L30	40 k	20 k	500	12 k

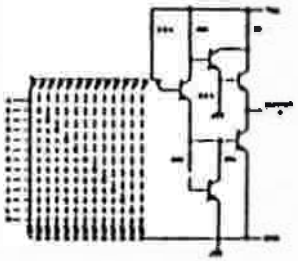
'00, '04, '10, '20, '30
'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS
Input clamp diodes not shown



'H00, 'H04, 'H10, 'H20, 'H30 CIRCUITS



'LS00, 'LS04, 'LS10, 'LS20, 'LS30 CIRCUITS



'S00, 'S04, 'S10, 'S20, 'S30, 'S133 CIRCUITS

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '08,			SERIES 54H SERIES 74H 'H11, 'H21			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S08, 'S11			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					-800			-500			-400			-1000	μA
Low-level output current, I_{OL}		54 Family			16			20			4			20	mA
		74 Family			16			20			8			20	
Operating free-air temperature, T_A		54 Family	-55		125	-55		125	-55		125	-55		125	°C
		74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '08			SERIES 54H SERIES 74H 'H11, 'H21			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S08, 'S11			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = -18 mA					-1.5			-1.5			-1.5			-1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX		54 Family	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = MAX	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1						1	mA
					V_I = 7 V									0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50							μA
					V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			-1.6			-2			-0.4				mA
					V_{IL} = 0.5 V												-2	
I_{OS}	Short-circuit output current*	6	V_{CC} = MAX		54 Family	-20		-55	-40		-100	-20		-100	-40		-100	mA
					74 Family	-18		-55	-40		-100	-20		-100	-40		-100	
I_{CC}	Supply current	7	V_{CC} = MAX															

supply current†

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'08	11	21	20	33	3.88
'H11	18	30	30	48	8
'H21	12	20	20	32	8
'LS08	2.4	4.8	4.4	8.8	0.86
'LS11	1.8	3.6	3.3	6.6	0.85
'LS21	1.2	2.4	2.2	4.4	0.85
'S08	18	32	32	57	9.25
'S11	13.5	24	24	42	9.25

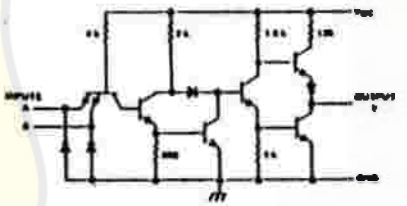
†Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

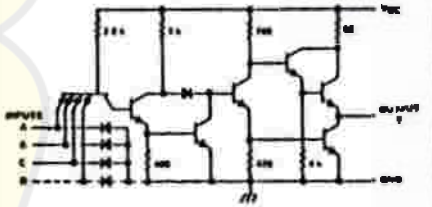
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C_L = 15 pF, R_L = 400 Ω		17.5	27		12	19
'H11, 'H21	C_L = 25 pF, R_L = 280 Ω		7.6	12		8.8	12
'LS08, 'LS11 'LS21	C_L = 15 pF, R_L = 2 kΩ		8	15		10	20
'S08, 'S11	C_L = 15 pF, R_L = 280 Ω		4.5	7		5	7.5
	C_L = 50 pF, R_L = 280 Ω		6			7.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

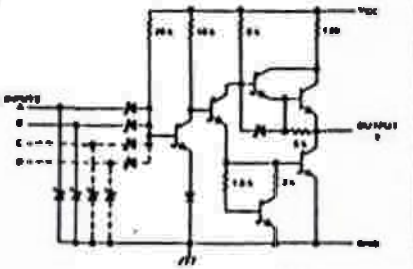
schematics (each gate)



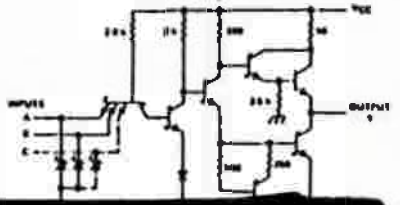
'08 CIRCUITS



'H11, 'H21 CIRCUITS



'LS08, 'LS11, 'LS21 CIRCUITS



8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easin[illegible] Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It [illegible] 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the fi[illegible] mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the seco[illegible] mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for ha[illegible] shaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which use[illegible] lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

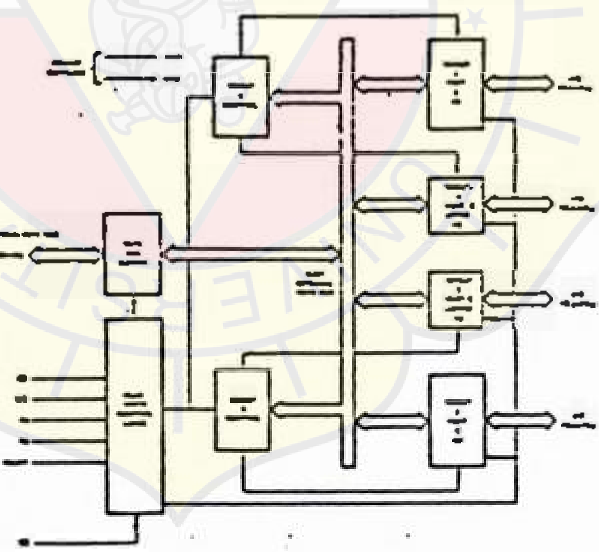


Figure 1. 8255A Block Diagram

Figure 2. Pin Configurat[illegible]

8255A /8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system. The functional configuration of the 8255A is programmed by systems software so that no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and issues commands to both of the Control Groups.

$\overline{(CS)}$

Chip Select. A "low" on this input pin enables communication between the 8255A and the CPU.

$\overline{(RD)}$

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read" from the 8255A.

$\overline{(WR)}$

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	X	1	0	PORT A – DATA BUS
0	1	0	1	0	PORT B – DATA BUS
1	0	0	1	0	PORT C – DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS – PORT A
0	1	1	0	0	DATA BUS – PORT B
1	0	1	0	0	DATA BUS – PORT C
1	1	1	0	0	DATA BUS – CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS – 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS – 3-STATE

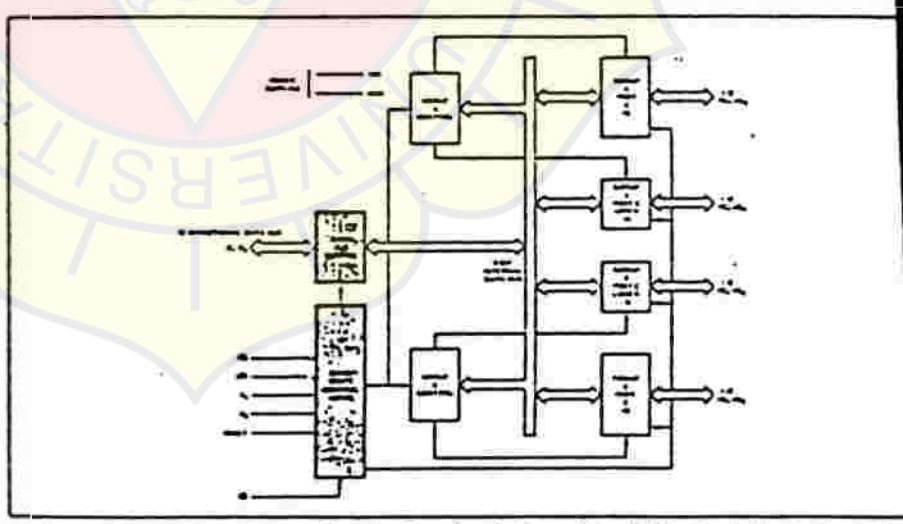


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

(RESET)

Reset. This ... on this input clears the control register and all ports (C, C) are set the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "... reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic ... "control words" ... from the internal data bus and ... the proper commands to its associated ports.

Control Group A — Port A and Port C upper (C7 - C4)
Control Group B — Port B and Port C lower (C3 - C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and ... can be configured in a wide variety of functional ... teristics by the system software but each has ... special features or "personality" to further enhance ... power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one ... data input latch.

Port B. One 8-bit data input/output latch/buffer and ... 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one ... data input buffer (no latch for input). This port c... divided into two 4-bit ports under the mode co... Each 4-bit port contains a 4-bit latch and it can be... for the control signal outputs and status signal inp... conjunction with ports A and B.

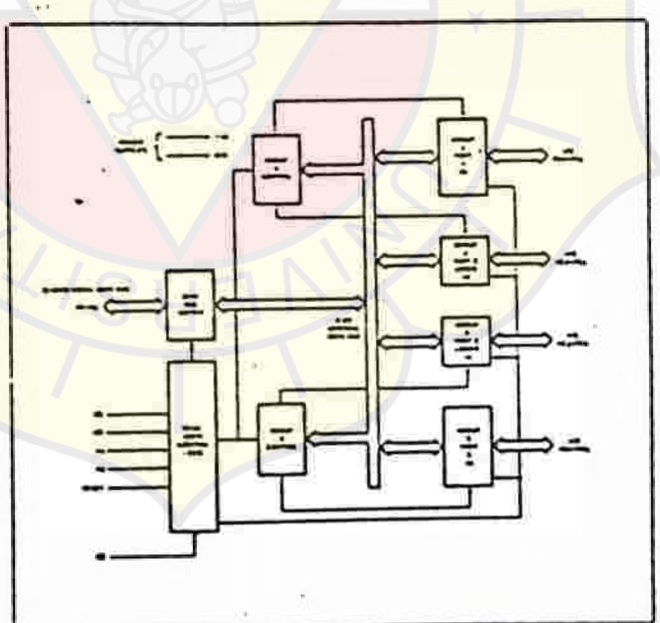
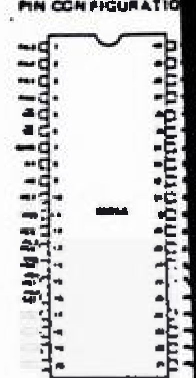


Figure 8225 A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D7-D0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
Vcc	+5 VOLTS
GND	0 VOLTS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic Input/Output
Mode 1 — Strobed Input/Output
Mode 2 — Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

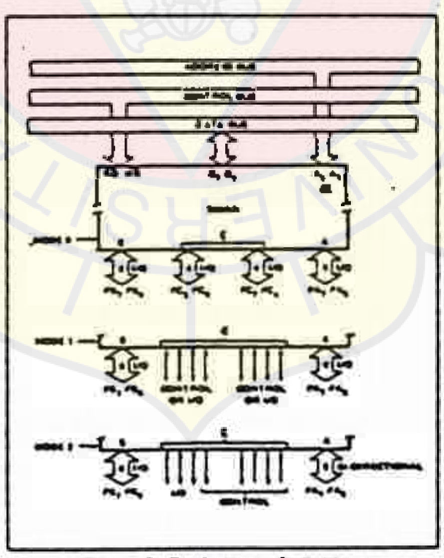


Figure 5. Basic Mode Definitions and Bus Interface

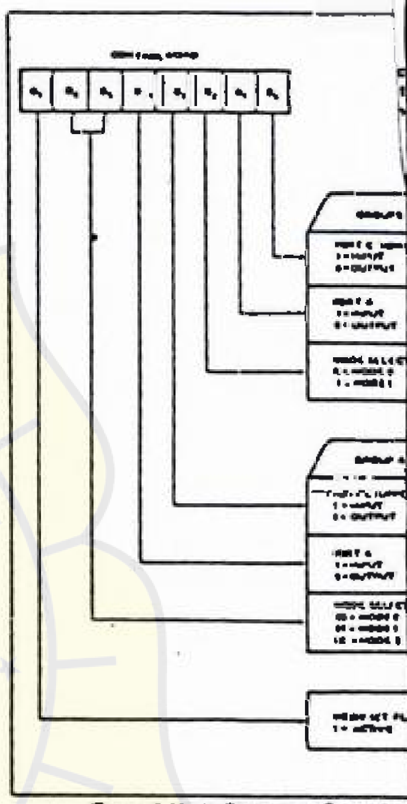


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

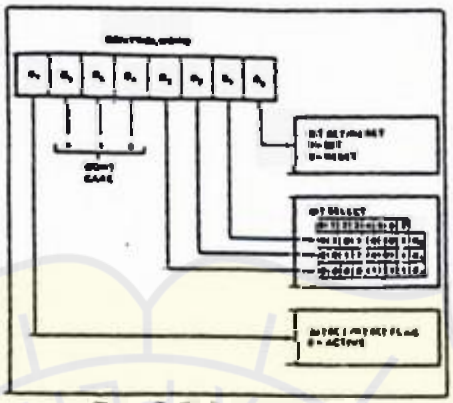


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for P
these bits can be set or reset by using the Bit Se
operation as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in
mode 2, control signals are provided that can
interrupt request inputs to the CPU. The int
quest signals, generated from port C, can be m
enabled or disabled by setting the associated
flop, using the bit set/reset function of port C

This function allows the Programmer to disallow
specific data transfers from interrupting the CPU witho
any other device in the interrupt structure.

The INTE flip-flop operation:

(BIT-SET) – INTE is SET – Interrupt enable
(BIT-RESET) – INTE is RESET – Interrupt

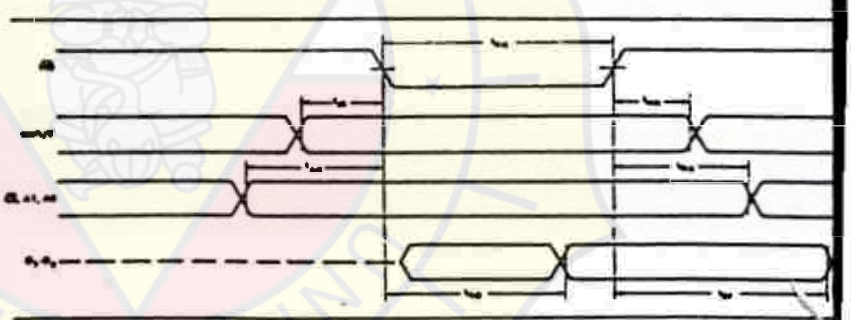
Note: All flip-flops are automatically r
mode selection and device Reset.

Operating Modes

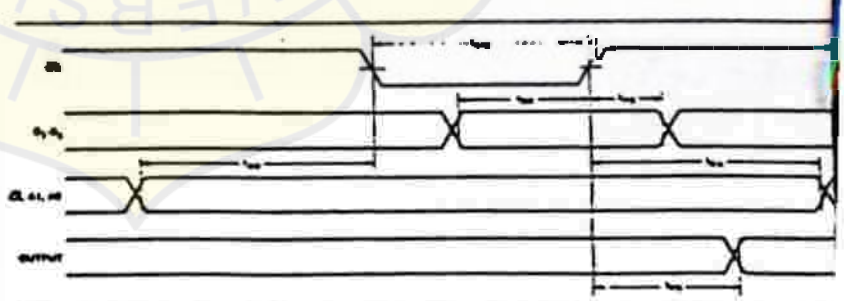
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required. data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are in this Mode.

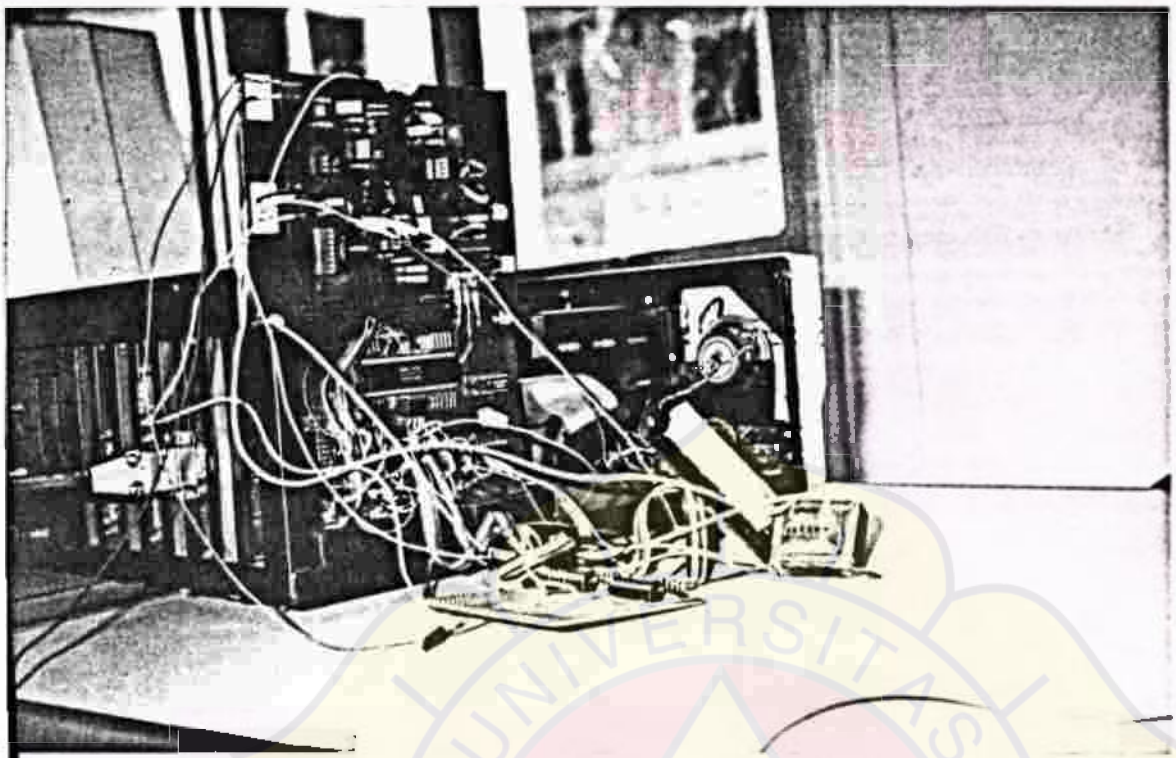


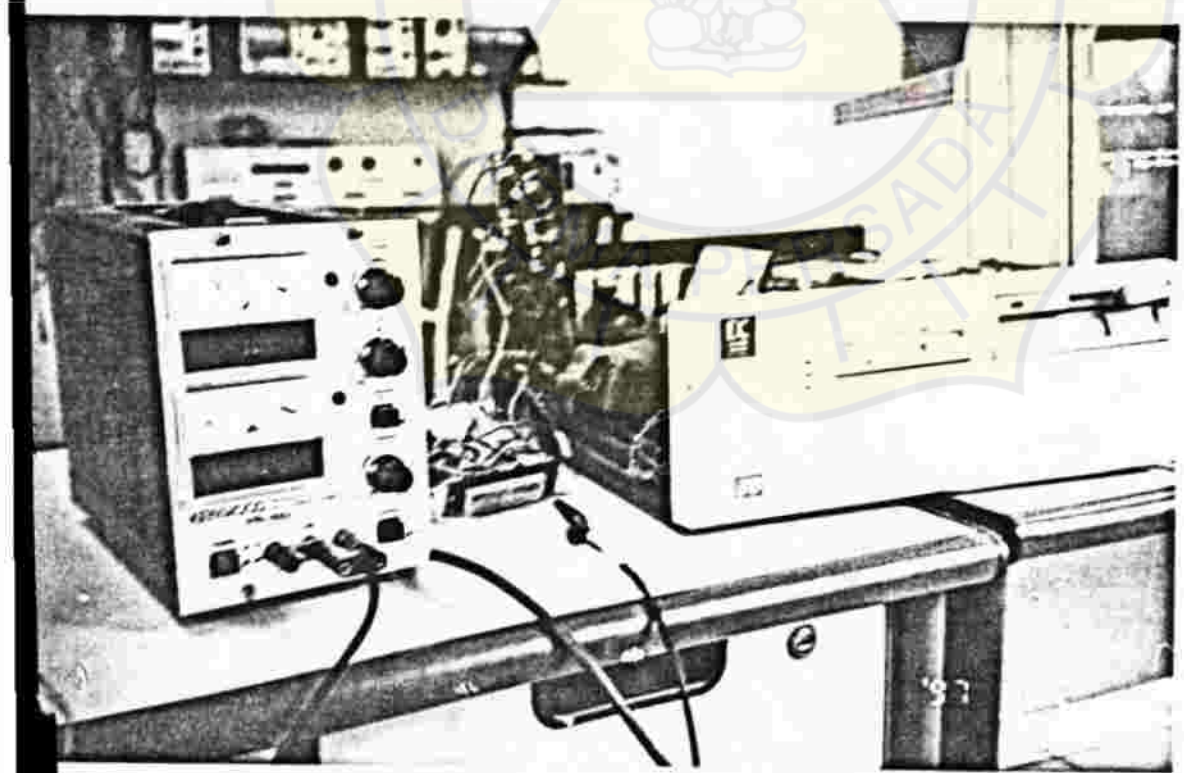
MODE 0 (Basic Input)



MODE 0 (Basic Output)


'97 9 2





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Jakarta, Agustus 1997

Andy Sofyan